DIGITAL SYMBOL GENERATOR 33

COPY NO. 0043

PREFACE

This manual is intended for use with the Type 30G and Type 30H Precision CRT Displays. These displays are identical in operation and circuitry and only differ in slight degree with respect to their use. The Type 30H contains six emitter followers and BNC connectors which allow an external oscilloscope to be used for monitoring purposes.

Engineering drawings and schematics may become outdated over a period of time. If the particular equipment does not completely resemble the printed drawing or schematic, please request a correct print for your particular equipment listing all model and/or serial numbers.

CONTENTS

SECTION 1

DESCRIPTION

	Page
General	1-1
Physical	1-1

SECTION 2

INTERFACE SIGNALS

Signal Description	2-1
Input Signals	2-1
Output Signals	2-3

SECTION 3

LOGICAL OPERATION

General	3-1
Numerical Conventions	3-1
Symbolic Conventions	3-1
Basic Operation	3-1
Symbol Generating Mode	3-5
Starting Location	3-5
Coordinate Circuit Operation	3-7
Intensity Level and Status Control Circuit	3-10
Status Signals	3-13
Format Determination	3-14
Symbol Matrix Generation	3-19

SECTION 4

MAINTENANCE

Electrical Adjustments	4-1
Delays	4-1
Character Size	4-1
Subscript Drop	4-2
Troubleshooting	4-2

SECTION 5

DIAGRAMS

		Page
	Cable Schedule	5-2
	Wiring Schedule	5-12

ILLUSTRATIONS

Figure		
1-1	Type 30 Precision CRT Display	vi
1-2	Logic Panel and Power Supply Locations	1-4
3-1	DEC Logic Symbols	3-3
3-2	Type 33 Digital Symbol Generator Block Diagram	3-4
3-3	Symbol Matrix Format	3-5
3-4	X Counter and Y Buffer Logic Block Diagram	3-9
3-5	Intensity Level and Status Control Logic Block Diagram	3-11
3-6	Subscript Logic Block Diagram	3-15
3-7	Character Size Logic Block Diagram	3-17
3-8	Increment and Space Control Logic Block Diagram	3-18
3-9	Timing Control Logic Block Diagram	3-20
3-10	Matrix Sequencer Logic Block Diagram	3-23
3-11	Sequencer Control Logic Block Diagram	3-27
3-12	Deflection Modifier Logic Block Diagram	3-28
3-13	18-Bit Shift Register Logic Block Diagram	3-29

TABLES

Table		
1-1	Operating Specifications	1-2
1-2	Physical Specifications	1-5
2-1	Interface Signals from PDP-1	2-1
2-2	Interface Signals from PDP-4	2-2
2-3	Interface Signals to PDP-1	2-3
2-4	Interface Signals to PDP-4	2-4
3-1	Starting Coordinate Loading Program for PDP-1	3-6
3-2	Starting Coordinate Loading Program for PDP-4	3-7
3-3	Intensity Loading Program for PDP-4	3-12
3-4	Intensity Correlations	3-13
3-5	Format Loading Program for PDP-1	3-16
3-6	Format Loading Program for PDP-4	3-16
3-7	Symbol Generating Cycle Steps	3-26
5-1	List of Diagrams	5-1

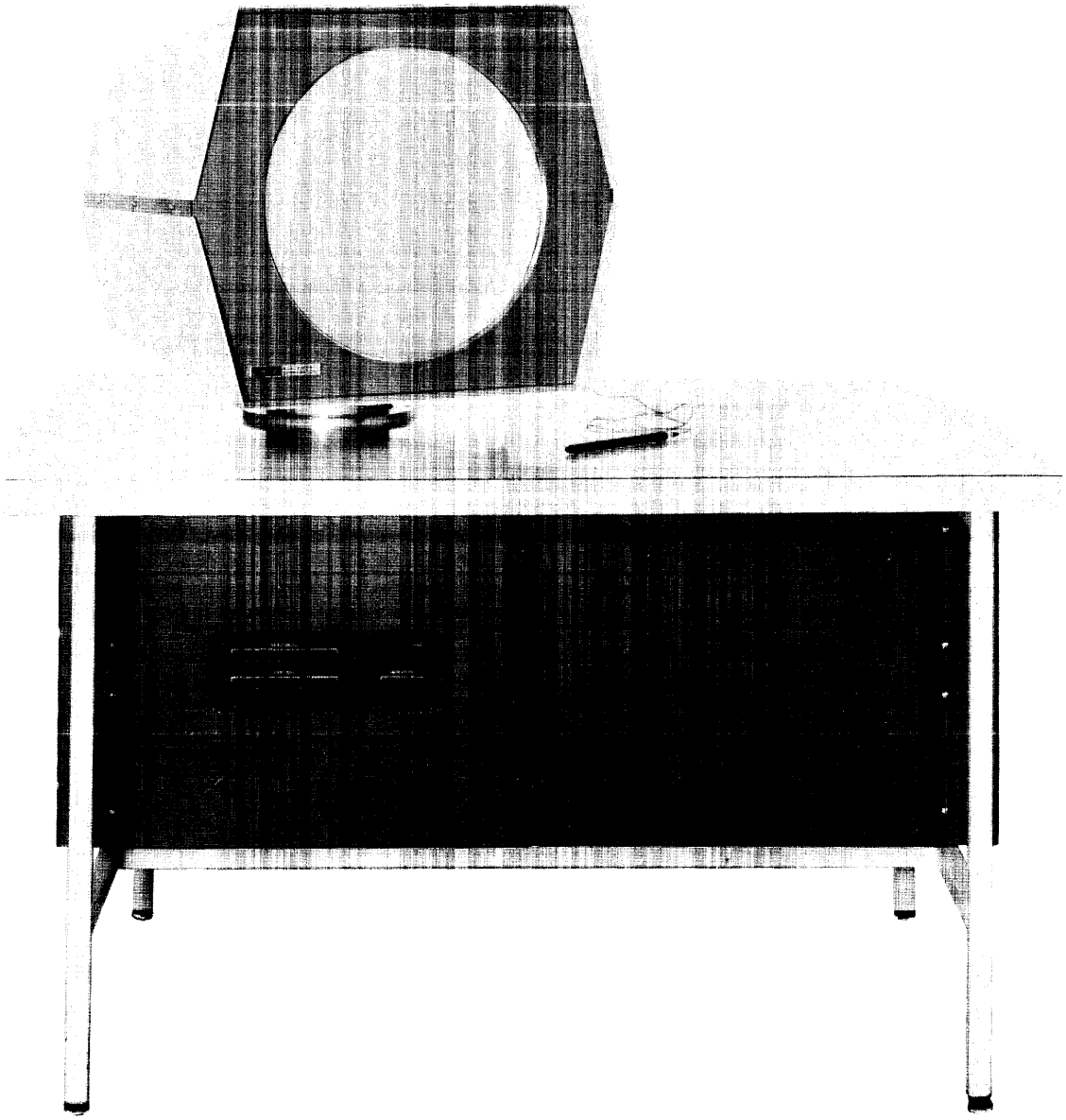


Figure 1-1 Type 30 Precision CRT Display

SECTION 1

DESCRIPTION

GENERAL

The Type 33 Digital Symbol Generator is an ancillary item designed and manufactured by Digital Equipment Corporation for use with their PDP-1 and PDP-4 computers. It is used in conjunction with either a Type 30G or a Type 30H Precision CRT Display to present alphanumeric symbols on the CRT with a minimum of computer time and programming. The operation of the display is unaffected in its normal point plotting mode.

The Type 33 controls the operation of the display in the symbol generating mode. It enables the display to show any symbol that can be made with a 5 by 7 dot matrix, at any selected location on the raster. Once a location has been selected, symbols are automatically positioned on a horizontal line, and each succeeding symbol is automatically moved one position to the right. Any symbol can be dropped to a subscript position at any location with no extra commands. A separate format command is used to select one of four matrix sizes and to space one position to the right.

The display itself uses two 10-bit binary words and a display command to show a single dot at some location within a 1024 by 1024 dot square raster. Successive dots may be displayed at any random position at a 20 kilocycle rate. Eight different levels of intensity can be selected by the computer in both the point plotting and symbol generating modes.

The Type 30G may be used with either the PDP-1 or PDP-4 computers, while the 30H may be used only with the PDP-1. Aside from a few minor circuit changes to accomodate the different interface, the Type 30H has the ability to duplicate its presentation on an auxiliary high-speed oscilloscope such as the Tektronix RM 503. Both displays can use a Light Pen, either Type 32 or Type 370, to identify specific displays, and operate with either centered or offset rasters. Table 1-1 lists the operating characteristics of the Type 33 with either display.

PHYSICAL

The Type 33 Symbol Generator is an integral part of either a Type 30G or Type 30H Precision CRT Display. It occupies slightly more than one rack of logic circuits in the display and normally is not visible.

TABLE 1-1 OPERATING SPECIFICATIONS

Input Power	115 ± 10 volts, 60 cycles, single phase, at 8 amps.
Power Control	Input power manually turned on and off by a toggle switch or a circuit breaker, and remotely by a - 15 volt 5 milliampere signal.
Ambient Temperature	50° F (10° C) to 110° F (43° C).
Cathode Ray Tube	16ADP7A .
Focus	Magnetic .
Spot Size	Approximately 0.030 inch, 0.015 inch at the half-light output points.
Deflection	Magnetic. The electron beam is deflected by the earth's magnetic field, therefore the CRT housing should not be moved while spot positions are being made.
Deflection Sensitivity	0.009 inch change for change of least-significant bit in address, using 9-3/8 inch raster.
Stability of (0,0) Point	± 0.5% of raster size.
Stability of Deflection System	± 0.5% of raster size.
Overall Accuracy	± 3% of raster size overall, ± 1% of raster size not including distortion due to geometry of the tube and deflecting system.
Repeatability	± 0.05 inch regardless of the location of the preceding point.
Addressing Scheme	1's complement, with 2's complement possible. Horizontal zero may be at the center or on the left edge. Vertical zero may be at the center or on the bottom edge.
Raster Size	9 3/8 inches per side, with 1024 points per side.
Pincushion Distortion	Less than 3/16 inch per side.
Symbol Matrix	7 dots high by 5 dots wide.
Matrix Sizes	Dots may be spaced 2, 3, 4, or 5 points apart. Overall matrix is either: (1) 0.13 by 0.09 inch (2) 0.19 by 0.14 inch (3) 0.26 by 0.18 inch (4) 0.32 by 0.23 inch
Subscript Drop	Adjustable from 0 to 100% of matrix size.
Intensity Levels	8 distinct levels selected by the octal number of a 3-bit word.
Single Display Time	3 microseconds from application of coordinate address words to display command, 35 microseconds for deflection setup delay, and 3 microseconds for intensification

TABLE 1-1 OPERATING SPECIFICATIONS (continued)

Symbol Display Time	Approximately 96 microseconds from start of first memory cycle to end of display cycle, plus 3 microseconds for each dot intensified.
Format Loading Time	10 microseconds for 2 memory cycles.
Indicators	10 X-AXIS and 10 Y-AXIS indicators show the coordinate address of the spot from either the center or the lower left-hand corner of the symbol matrix. Three INTENSITY indicators give the octal number of the intensity level. An LPS indicator glows if the light pen saw a spot. The NAC indicator lights when the computer requests a completion pulse.
Controls	The only operator controls are the main power switch inside the power supply bay and light pen gain control underneath the front corner of the CRT housing.

The two items consist of a table with a 16-inch cathode ray tube (CRT) in a movable housing above the table top and two mounting bays underneath the table top. When viewed from the front, the CRT housing is on the left side of the table above 25 indicator lights visible through a cutout in the trim panel (see Figure 1-2).

The two mounting bays contain the dc power supplies and most of the electrical circuitry. Some circuitry is contained in the CRT housing. For location purposes the left-hand mounting bay is bay 1, and the right-hand mounting bay is bay 2. Bay 1 contains an indicator panel in the front and the majority of the logic circuits in the rear. Bay 2 contains the power control panel in the front and the three dc power supplies in the rear. These are divided into three horizontal rows; A at the top, B in the center, and C at the bottom (the logical circuits in the CRT housing are considered row D). The lower rows contain 25 vertical sockets, numbered from left to right. A socket in row A has the same number as the socket directly below it in row B. Each socket has 22 terminals designated from top to bottom by the letters of the alphabet (G, I, O, and Q are not used). Therefore, any terminal is specified by the module (socket) location and socket terminal. As an example, C10H is in bay 1 (understood because all modules are in bay 1), row C, tenth socket from left (tenth module from right if viewed from inside the bay), and is the seventh terminal down.

Some of the sockets have component mounting boards over their terminals; these are identified by the prefix CB- followed by the socket location. A few sockets have insulated stand-off

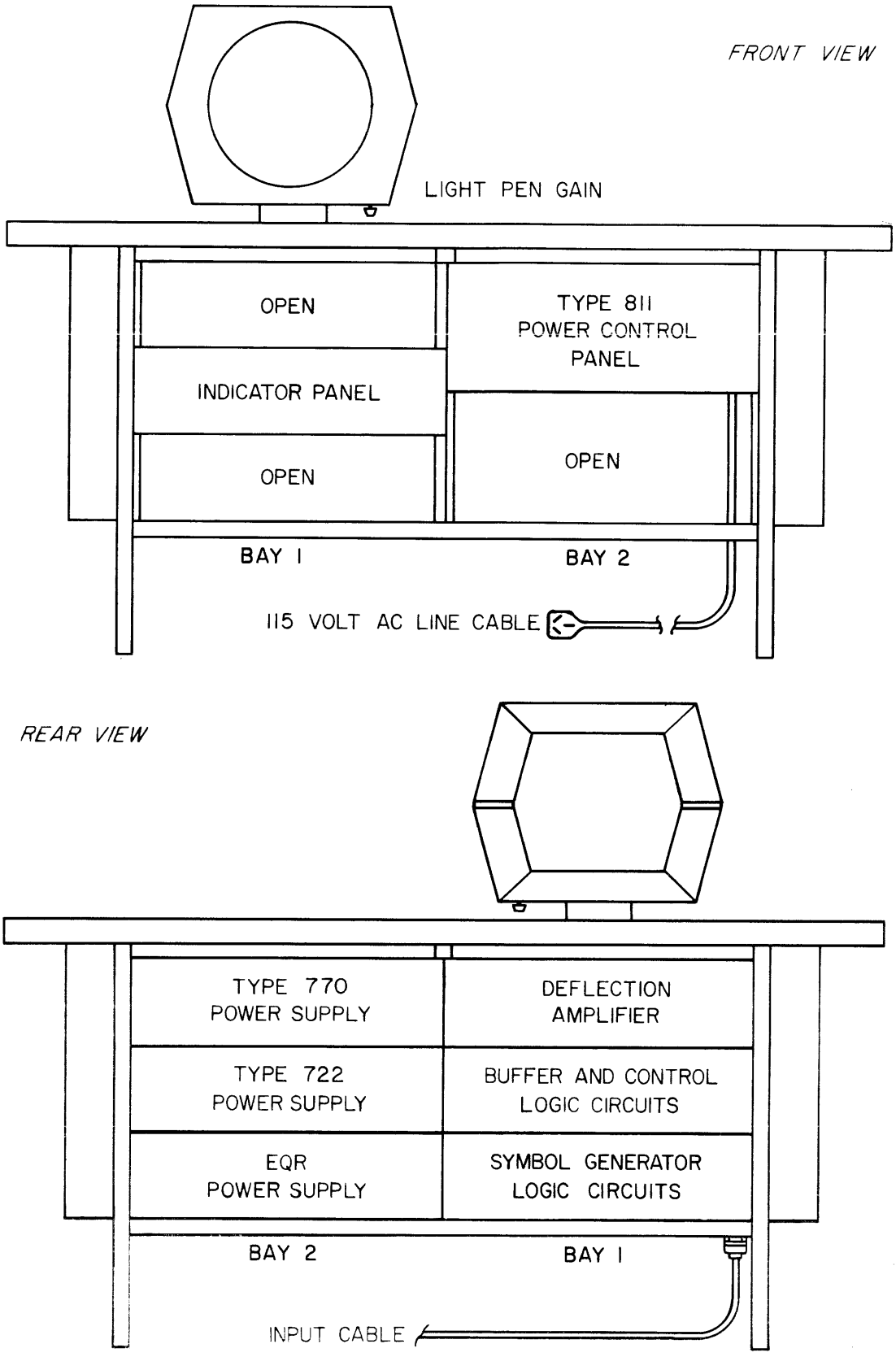


Figure 1-2 Logic Panel and Power Supply Locations

terminals above them; these are identified by the prefix ST- followed by the socket location. Two switches are mounted on brackets for centering or offsetting the zero point. The switch on the left is S1 for the horizontal axis, and the switch on the right is S2 for the vertical axis.

Rows A, B, and C are fastened to a sliding rack. The rack may be pulled out for access to the modules and cables. Rows B and C have a panel with three switches on its left-hand edge. These switches are used for testing the operation of the equipment under marginal power conditions. Under normal conditions they are down; throwing them up connects that bus to the marginal power supply (if connected). The upper switch controls the +10A bus to the A terminals, the center switch controls the +10B bus to the B terminals, and the lower switch controls the -15 bus to the C terminals. All the D terminals are ground.

TABLE 1-2 PHYSICAL SPECIFICATIONS

Dimensions	50 inches wide, 34 inches deep, 24 inch table height, 49 inches overall height.
Weight	Approximately 400 pounds.
Mounting	CRT assembly mounted to table, all logical circuits and power supplies mounted under the table. The table legs have adjustable feet for leveling, and normally support 100 pounds each when properly adjusted.
Clearance	Access room for maintenance requires 3 feet in front and rear and 2 feet above.
CRT Housing	Tilts approximately 5° forward and 20° backward, and rotates 60° sideways. Full 360° rotation possible by removing stop bolts. A 1/8-inch thick sheet of form-fitted plexiglass protects the face of the CRT.
Color	Blue and grey tweed unless otherwise specified.

The deflection output amplifiers and precision resistor stacks in row A are mounted on heat sinks which are cooled by muffin fans. The center fan also operates an airflow-actuated sail switch. This switch controls the application of ac power to the dc power supplies and must be closed before the equipment will operate.

The CRT housing rotates and tilts to allow a good optical presentation of the display. The housing contains the CRT; the mount for the CRT, deflection yoke, and focus coil; a four-module mounting box (row D); the CRT component mounting plate; and the light pen gain control potentiometer. The cables for the CRT go through the mounting pipe.

WARNING

Lethal voltages are present in this equipment. Never touch the black ring around the CRT near the front bezel (exposed on early models). Turn off all power before removing any modules.

CAUTION

An airflow-actuated sail switch controls the application of the 115-volt power to the equipment. Loss of cooling air will shut off the main power. Never operate the equipment without cooling air, as the deflection amplifier transistors will overheat. Replacement cost is approximately $600.

SIGNAL DESCRIPTION

All logic signals between the computer and the display are either Standard DEC Logic Levels or Standard DEC Pulses. A Standard DEC Logic Level is either a ground (0 to -0.3 volts), indicated by an open diamond (—◇), or -3 volts (-2.5 to -3.5 volts), indicated by a solid diamond (—◆). Dual-polarity level logic is used; therefore the particular voltage-logic state relationships are defined by individual usage. All logic levels that are applied to the conditioning level inputs of capacitor-diode gates must be present either 1 or 3 microseconds before an input triggering signal is applied to the gate. The Standard DEC Negative Pulse is indicated by a solid triangle (—▶) and goes from ground to -2.5 or -3 volts (-2.3 to -3.5 volt tolerances). The Standard DEC Positive Pulse, indicated by an open triangle (—▷), goes either from -3 volts to ground or from ground to +2.5 volts (+2.3 to +3.0 volts). The width of the standard pulses used in this equipment is either 1.0, 0.4, or 0.07 microseconds, depending on the module and application. All interface pulses are 400 nanoseconds wide. Any other signal is non-standard and is indicated by an arrowhead pointing in the direction of flow(—➤).

INPUT SIGNALS

The required input signals for the Type 33 are the same for either the Type 30G or 30H displays when used with a PDP-1, but are different when used with a PDP-4. Tables 2-1 and 2-2 list these signals by their mnemonic names and include a functional description. The term "Levels" means that DEC Standard Levels are required. The definition of logical states for these signals must be obtained from Section 3. The term "Pulse" means a DEC Standard 0.4-microsecond Negative Pulse is required. Two other inputs require a constant -15 volt level if used. Not listed is a variable dc voltage input used with the marginal voltage checks.

TABLE 2-1 INTERFACE SIGNALS FROM PDP-1

Mnemonic	Name/Description	Type
X_{0-9}	10 bits comprising the horizontal coordinate word.	Levels
SR_{0-17}	SR_{0-9} = vertical coordinate word, SR_{15-17} = format word.	Levels

TABLE 2-1 INTERFACE SIGNALS FROM PDP-1 (continued)

Mnemonic	Name/Description	Type
SR_{0-17}	SR_{0-16} = first half of character word, SR_{17} = subscript control signal. SR_{0-17} = second half of character word.	
DPY	DisPlaY. Enabling and control signal.	Level
INT-1 INT-2 INT-3	3-bit INTensity level word.	Levels
CDP	Clear Display Pulse. Clears flip-flops.	Pulse
LDP	Load Display Pulse. Loads coordinate and intensity words.	Pulse
RESET	Resets light pen status flip-flop.	Pulse
LDF	LoaD Format. Loads format word.	Pulse
PLT	PLoT. Starts symbol generation.	Pulse
RTO	Remote Turn On. Power control level.	-15 v
NAC	Need a Completion. Indication signal.	-15 v

TABLE 2-2 INTERFACE SIGNALS FROM PDP-4

Mnemonic	Name/Description	Type
SR_{0-17}	SR_{8-17} = horizontal coordinate word. SR_{8-17} = vertical coordinate word. SR_{15-17} = intensity level word. SR_{15-17} = format word. SR_{0-16} = first half of character word, SR_{17} = subscript control signal. SR_{0-17} = second half of character word.	Levels
DPY	DisPlaY. Enabling and control signal.	Level
CXB	Clear X Buffer. Clears horizontal counter.	Pulse
LXB	Load X Buffer. Loads horizontal coordinate word.	Pulse

TABLE 2-2 INTERFACE SIGNALS FROM PDP-4 (continued)

Mnemonic	Name/Description	Type
CYB	Clear Y Buffer. Clears vertical buffer.	Pulse
LYB	Load Y Buffer. Loads vertical coordinate word.	Pulse
CDI	Clear Display Intensity. Clears intensity buffer.	Pulse
LDI	Load Display Intensity. Loads intensity word.	Pulse
LDF	Load Display Format. Loads format word.	Pulse
PLT	PLoT. Starts symbol generation.	Pulse
RTO	Remote Turn On. Power control level.	-15 v
RESET	Resets light pen status flip-flop.	Pulse

OUTPUT SIGNALS

The output signals produced are different for each computer and display combination. These signals are either DEC Standard Levels or 0.4 microsecond pulses, or are non-standard intensity level and timing signals and analog deflection signals from emitter followers that are used to control a remote slave display. These signals are listed in Tables 2-3 and 2-4.

TABLE 2-3 INTERFACE SIGNALS TO PDP-1

Type 33 with Type 30G Display		
Mnemonic	Name/Description	Type
DDP	Display Done Pulse. Occurs at end of point plotting mode and after each half of a symbol generating operation.	Pulse
LPF	Light Pen Flag. Occurs when the light pen sees a displayed spot.	Pulse
LPS	Light Pen Status. Goes to -3 volts when the light pen sees a spot until reset from the computer.	Level

TABLE 2-3 INTERFACE SIGNALS TO PDP-1 (continued)

Type 33 with Type 30H Display		
Mnemonic	Name/Description	Type
DDP	Display Done Pulse.	Pulse
LPF	Light Pen Flag.	Pulse
LPS	Light Pen Status.	Level
INT_{1-3}	Intensity buffer word.	Levels
INT-A	Intensify command. Three microsecond negative pulse when the CRT is to be unblanked.	Pulse
V_H	Horizontal deflection analog voltage.	Analog
V_X	Horizontal reference analog voltage.	Analog
V_V	Vertical deflection analog voltage.	Analog
V_S	Vertical reference analog voltage.	Analog

TABLE 2-4 INTERFACE SIGNALS TO PDP-4

Mnemonic	Name/Description	Type
DDP	Display Done Pulse.	Pulse
DDL	Display Done Level. Goes to -3 volts when DDP occurs until next CDP or PLT pulse occurs.	Level
LPS	Light Pen Status.	Level

SECTION 3
LOGICAL OPERATION

GENERAL

The basic operation of the Type 33 Digital Symbol Generator is the same, whether a Type 30G or a Type 30H Precision CRT Display is used with it, or whether it is controlled by a PDP-1 or a PDP-4. The Type 33 has two modes of operation: a single, random-position, point plotting mode; and a symbol generating mode. The point plotting mode of operation is very similar to the operation of the Type 30E; therefore it is not described in detail in this manual. The minor differences, however, are completely covered.

Numerical Conventions

In describing the operation of this equipment, three numerical systems are used: the binary (radix of 2), the octal (radix of 8), and the decimal (radix of 10). When using the decimal system, arabic numerials are used and the radix omitted, a 10 being understood. Similarly, the radix 2 is not shown on binary numbers as they consist entirely of zeros and ones and generally cannot be misunderstood. However, all octal numbers will be designated as such with a subscript 8 following the number.

Symbolic Conventions

Digital Equipment Corporation uses a drawing system in which the logical function, circuit location, trouble shooting, and wiring information are contained on a single drawing. Most general types of logical circuits are specified by a unique combination of shape, input and output connections, and internal nomenclature. The module type and location information are contained within the logical circuit symbol, if possible, or else within a dotted line around the circuit symbol. Input and output terminal designations appear next to the circuit symbol, and all external components are shown with their values. The assertive signal condition that produces the desired output is designated by a signal symbol. These symbols may be either logic 1 or logic 0 as dual-polarity level logic is used. The various symbols used in the Type 33 are depicted in Figure 3-1. Names of signals that go through the interface are given in capital letters, while internal signal names are given in lower case letters.

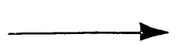
BASIC OPERATION

The basic operation of the Type 33 can most easily be understood by referring to the logical

block diagram, Figure 3-2. This diagram shows the configuration of the Type 33 and Type 30G with both the PDP-1 and PDP-4 options. The only difference when using the Type 30H is the addition of some emitter followers that make the analog voltage inputs to the deflection amplifiers and the intensification signal from the timing control available for external use. Three intensity buffer inverters for use with the PDP-1 are not shown.

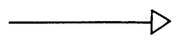
Point Plotting Mode - In the point plotting mode, a spot of light is displayed on the screen of the CRT for 3 microseconds somewhere within a 9-3/8 inch square raster in each display cycle. The location of the spot is controlled by four currents flowing through a deflection yoke, and is directly related to the numerical value of two 10-bit binary words. The computer loads one of these binary words into the Y buffer, and the other into the X counter (which acts as a buffer). The voltage of each bit in both of these words is amplified and standardized, and then each word is converted into an equivalent analog voltage by a digital-to-analog converter. Each analog voltage controls the current through two opposing deflection coils in the deflection yoke, whose resultant magnetic field deflects the electron beam to its preselected point. The spot is not produced until 35 microseconds after the binary words are loaded into the buffers to eliminate any movement of the spot. The IOT command in the PDP-1 that transfers the two words to the buffers and initiates the display cycle also selects the level of intensity of the displayed spot. With the PDP-4, each loading of the coordinate words and the intensity word requires a separate IOT command.

Symbol Generating Mode - Operation in the symbol generating mode is more complicated. The computer determines the location of the left end of a horizontal line along which symbols are to be plotted and loads this location into the X counter and Y buffer as in the point plotting mode, but does not initiate the 35-microsecond setup delay or permit a display. It next determines the intensity level, whether incrementing for additional symbols is needed, and the character size format for the line; and loads this information into the intensity and format buffers. Then it selects the first half of the particular symbol word to be generated and determines if it is to be a subscript, and loads this into a shift register with a command that initiates the symbol matrix plotting sequence. The computer must now select the last half of the symbol word and wait for the Type 33 to give a completion signal when the first half of the symbol word has been displayed, then transfer the last half of the symbol word to the shift register with a command that starts the symbol matrix plotting sequence again from the place where it left off. The Type 33 will again return a completion signal to the computer when it has finished displaying the character and has incremented the X counter to the beginning location of the next symbol.

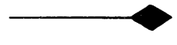


Miscellaneous signal. Indicates direction only. No voltage levels or timing considerations implied.

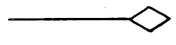
DEC negative-going 3 volt pulse, usually from ground to -2.5 volts. Pulse widths of 70,400, and 1000 nanoseconds.



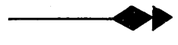
DEC positive-going 3 volt pulse, usually from -3 volts to ground. Pulse widths of 70,400, and 1000 nanoseconds.



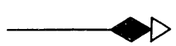
Negative level, -3 volts. Greater than one microsecond.



Positive level, ground. Greater than one microsecond.

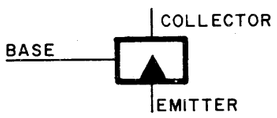


Negative-going level which triggers on its leading edge, or differentiates. Open diamond and arrow for positive-going levels.

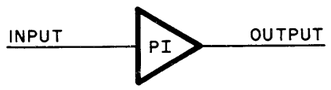


Negative-going level which triggers on its trailing edge. Open diamond and solid arrow for positive-going levels. Also applicable to pulses.

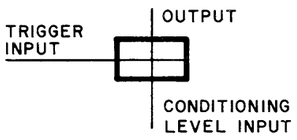
Clamped load resistor. Normally goes to -15 volts, with the output clamped to -3 volts. Gives ground and -3 volts output pulses or levels.



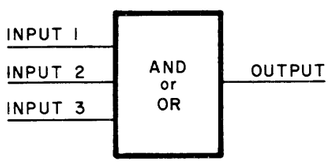
Inverter. A transistor in common-emitter configuration, with biased input on its base. Emitter must be at ground to conduct. Ground input cuts it off and -3 volt input saturates it. Delay = 20 nanoseconds.



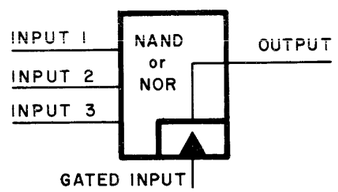
Pulse Inverter. Similar to standard inverter but with lower driving power. Used only with Capacitor-Diode Gates.



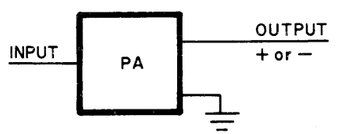
Capacitor-Diode Gate. Differentiates the input if the conditioning level has had the proper voltage on it for approximately 3 microseconds. No delay between input and output pulses.



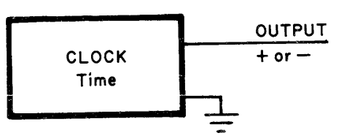
Logic Gate. May be either AND or inclusive OR, depending on polarity of inputs and output. Number of inputs unlimited.



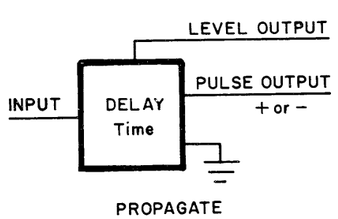
NAND or NOR Logic Gate. Same as an AND or OR Logic Gate with an inverter which may be gated. Output polarity opposite to input polarities.



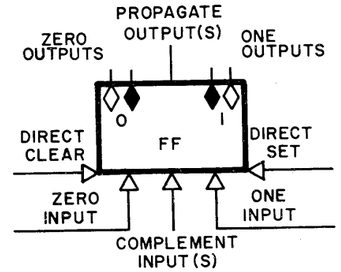
Pulse Amplifier. Amplifies and standardizes DEC pulses. Output is from a pulse transformer, giving either positive or negative pulses depending on which side is grounded.



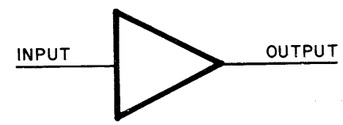
Clock. An astable multivibrator that generates a continuous series of DEC pulses. May be of either polarity. Frequently crystal controlled.



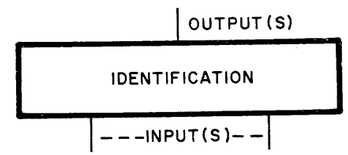
Delay. A monostable multivibrator which produces one or two level outputs while it is timing out, and then may trigger a Pulse Amplifier. Operating time adjustable.



Flip-Flop. A bistable multivibrator with numerous inputs and two outputs, which may be buffered. Outputs shown twice, with diamonds indicating voltage levels in each state. Positive pulses from ground to +2.5 volts are required on inputs to set or clear the flip-flop. A complement input changes the state regardless of the previous state, and may generate a propagate pulse output.

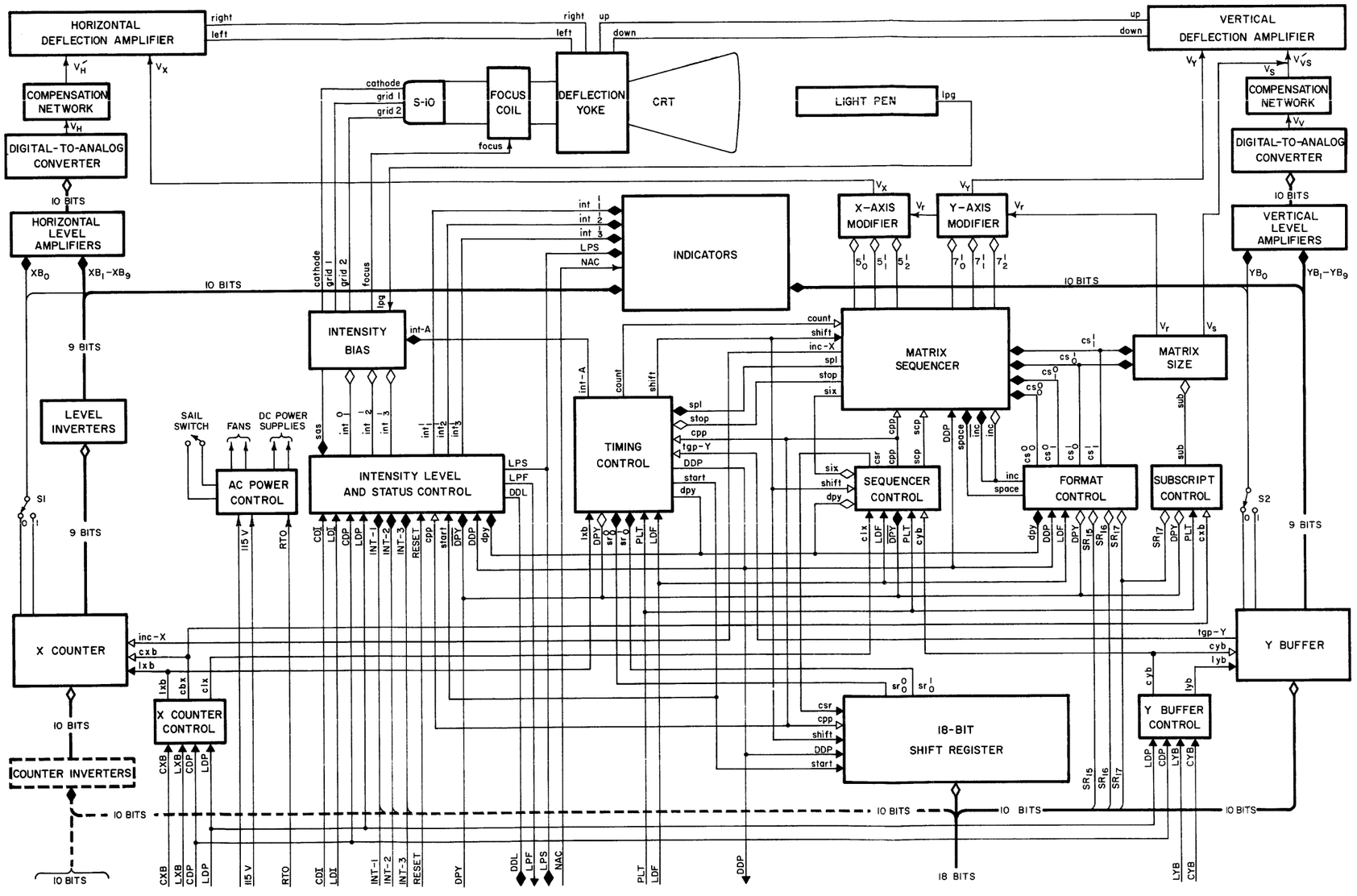


Analog Amplifier. Any amplifier that operates over a continuous voltage range. May have single or multiple inputs and/or outputs. Generally requires different voltages.



Other types of circuits, such as Digital-to-Analog Converters, Electronic Switches, Switch Filters, Level Amplifiers, etc. Shown in any shape or orientation.

Figure 3-1 DEC Logic Symbols



NOTES:

1. Configuration shown using the Type 30G Precision CRT Display. When used with the PDP-1, the vertical address word is applied to the X counter directly and the counter inverters and three intensity inverters (not shown) are used. When used with the PDP-4, both address words are from the same AC register as the symbol words.
2. The configuration for using the Type 30H Precision CRT Display is the same with the addition of emitter followers and BNC connectors for V'_H, V_X, V_Y, V'_{VS}, INT-A, and INT-B.

Figure 3-2 Type 33 Digital Symbol Generator Block Diagram

SYMBOL GENERATING MODE

The Type 33 automatically generates a 5 by 7 matrix of some predetermined size with the lower left corner at a predetermined starting location. It moves the position of the electron beam in sequential increments from 0 to 34 as shown in Figure 3-3, with 2 microseconds required for each move. A symbol is generated by intensifying the electron beam for 3 microseconds when it is located at the desired position. This requires two 18-bit words per symbol from the computer, with a 1 in each bit for an intensified location and a 0 in each bit for a blanked location. The extra bit, 17 in the first half of the symbol word, is not displayed but is used as a control level to select normal or subscript locations for the matrix.

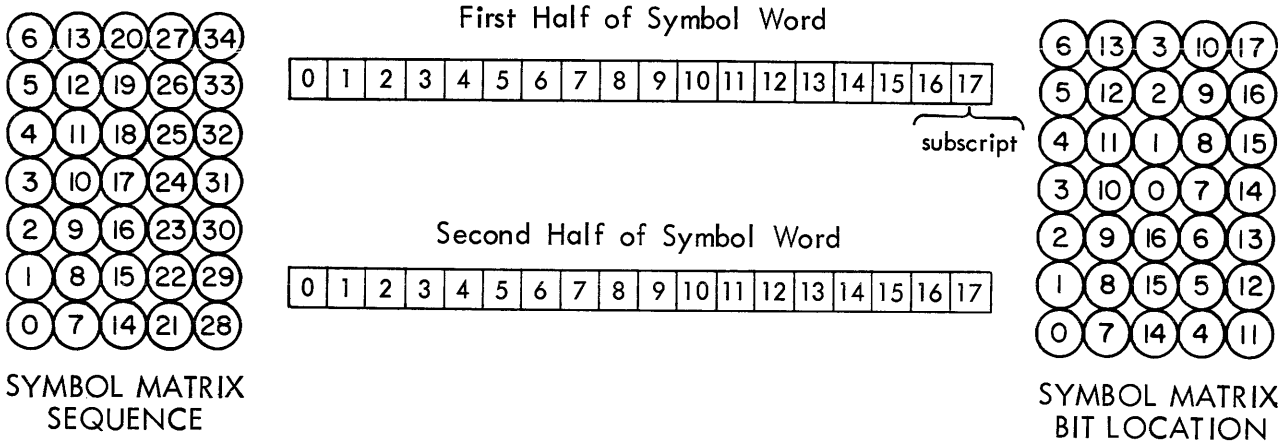


Figure 3-3 Symbol Matrix Format

Starting Location

Before a symbol or line of symbols can be displayed, it is necessary to specify the location of the lower left corner of the first symbol on the line. This is accomplished by having the computer load the X coordinate of the location into the X counter and the Y coordinate of the location into the Y buffer. Because two different computers are used, the coordinates are loaded in two different manners.

PDP-1 Coordinate Loading - The PDP-1 has two registers available for in-out transfer of digital information, as well as a register that makes some of the bits of the in-out transfer (IOT) command available as control levels. This makes it possible for both coordinate address words and all necessary control pulses and levels to be transferred to the Type 33 during the two memory

cycles of the IOT operation. However, each of the two registers - the accumulator (AC) and the input-output (I-O) - must be loaded from memory separately before the IOT command. Each loading operation takes two memory cycles; so a total of 30 microseconds is necessary for the computer to retrieve the coordinate address words and loading command from memory and effect their transfer to the Type 33. The three program steps necessary are listed in Table 3-1.

TABLE 3-1 STARTING COORDINATE LOADING PROGRAM FOR PDP-1

Mnemonic Name	Code Number (octal)	Time (μsec)	Operation	Explanation
lac X	20xxxx	10	C(xxxx) ⇒ C(AC)	X coordinate word in xxxx loaded into AC
lio Y	22yyyy	10	C(yyyy) ⇒ C(I-O)	Y coordinate word in yyyy loaded into I-O
sdb	722007	10	C(AC) ⇒ C(XC) C(AC) ⇒ C(YB) no display	All display buffers cleared, X coordinate word transferred into X counter, Y coordinate word transferred into Y buffer, deflection setup delay and intensification inhibited, intensity buffer loaded for normal intensity level

Only the first ten bits of the AC register, AC_{0-9}, are used for the X coordinate word. The AC_{1-9} bits are ground for logic O and -3 volts for logic 1; therefore each of these bits must be inverted before application to the X counter. The first ten bits of the I-O register, $I\text{-}O_{0-9}$, are used for both the Y coordinate word and as part of the character word. The I-O register bits are -3 volts for logic O and ground for logic 1. The IOT command produces a clear display pulse (CDP) at TP_7 and a load display pulse (LDP) at TP_{10}, and makes bit 7 and bits 9, 10, and 11 of the command available from the memory buffer (MB). Bit 7 (MB_7) is the display (DPY) level, permitting a display when it is a logic O (MB_7^0) and inhibiting a display when it is a logic 1 (MB_7^1). The other three bits control the intensity level, which is normal when their octal number is 0. Increasing the number to 3_8 progressively increases the intensity, while 4_8 drops it to the minimum value. Further increases slowly raise the intensity towards normal again. These bits form the third digit from the right in the instruction word.

PDP-4 Coordinate Loading - The PDP-4 only has one 18-bit register, the accumulator (AC), for transfer of information between an external device and the computer, as well as the memory buffer which makes some of the bits of the IOT command available as control levels. Each

coordinate address word must therefore be loaded into a buffer in the Type 33 individually. In addition, the intensity buffer is loaded with the same bits as the format buffer; so each of these requires separate loading operations. This makes three separate pairs of clear and load pulses necessary, whereas the PDP-1 only requires one pair.

All 18 bits from the AC register are applied to the inputs of the shift register. The ten less-significant bits (AC_{8-17}) are used for both the X and Y coordinate address words, while the three less-significant bits (AC_{15-17}) are used for both the intensity and format words. The counter inverters shown in Figure 3-2 are not used, nor are the three inverters of the intensity buffer (not shown).

The PDP-4 has an 8-microsecond memory cycle, during which it can produce various output pulses at TP_1, TP_5, and TP_7. Like the PDP-1 it requires two memory cycles to retrieve a word from memory and load it into the AC register, but only one memory cycle is needed to effect an IOT command. Since the two coordinate words are loaded separately, a total of 48 microseconds is required for retrieval and transfer of the starting coordinate. The four program steps necessary are listed in Table 3-2.

TABLE 3-2 STARTING COORDINATE LOADING PROGRAM FOR PDP-4

Mnemonic Name	Code Number (octal)	Time (μsec)	Operation	Explanation
lac X	20xxxx	16	C(xxxx) ⇒ C(AC)	X coordinate word in xxxx loaded into AC
dxl	700506	8	C(AC) ⇒ C(AC)	X counter cleared at TP_5, X coordinate word transferred into X counter at TP_7
lac Y	20yyyy	16	C(yyyy) ⇒ C(AC)	Y coordinate word in yyyy loaded into AC
dyl	700606	8	C(AC) ⇒ C(YB)	Y buffer cleared at TP_5, Y coordinate word transferred into Y buffer at TP_7

Coordinate Circuit Operation

The logic block diagrams for the X counter and X counter control, and the Y buffer and Y buffer control used by the Type 30G are shown in Figure 3-4. The Type 30H does not use the counter inverters and uses a Type 4218 Quadruple Flip-Flop module in the more-significant part of the Y counter instead of a Type 4213. The Type 4218 allows a jam transfer of the four more-significant bits of the vertical address to be effected without clearing the Y buffer, thereby

shortening the time required for large vertical spot movements. Four inverters are also needed to produce the dual logic levels per bit necessary for jam transfer.

The input connections for the X counter and Y buffer differ depending on whether a PDP-1 or a PDP-4 is being used. These connections are listed in the wiring tables in Section 5. The PDP-1 applies a negative clear display pulse (CDP) at TP_7 to pulse amplifiers in both the X counter and Y buffer control circuits. The X counter control circuit produces a negative 0.4-microsecond clear X (cls) pulse which generates a positive 1.0-microsecond clear X buffer (cxb) pulse and is used by the sequence control circuit to clear the matrix sequencer, timing control, and shift register circuits. The cxb pulse is applied to the direct clear input of all the X counter flip-flops and to the subscript flip-flop, setting them to their logic O states. The 1-microsecond pulse width is necessary to allow the carry propagate pulses to die out, insuring that the counter holds all zeros after the clear pulse.

The Y buffer control circuit produces a positive 0.4-microsecond clear Y buffer (cyb) pulse which is applied to all the direct clear inputs of the Y buffer flip-flops and is ORed with the clx pulse in the sequencer control circuit. In the Type 30H the cyb pulse is only applied to the six less-significant bit flip-flops as the jam transfer module does not require a separate clear pulse.

When the PDP-4 is used, it generates negative clear pulses at TP_5 on different IOT commands. Two clear pulses (CXB and CYB) are applied to the trigger inputs of capacitor-diode gates in the Type 4606 Pulse Amplifier modules. These gates are three-input OR gates with two direct pulse inputs and one capacitor-diode gate (permanently enabled by negative potentials on their conditioning level inputs). Operation after the particular IOT clear pulse occurs is identical to the PDP-1 operation previously described.

The PDP-1 normally produces a load display pulse (LDP) at TP_{10}, 2.2 microseconds after the CDP pulse. This pulse is applied to a Type 4606 Pulse Amplifier, producing the load X buffer (LXB) pulse. The lxb pulse loads the X coordinate word into the X counter, and triggers the point plotting mode in the timing control circuit (if specified by the display command, DPY). The lxb pulse is also produced by the LXB load pulse from the PDP-4 at TP_7.

The negative lxb pulse is applied to a pulse inverter in each X counter module, producing positive trigger gate pulses (tgp-x). These pulses are applied to the trigger inputs of positive capacitor-diode gates, each of which will differentiate the pulse if a ground potential has been on its conditioning level input for at least 3 microseconds. Since the PDP-1 has applied the bits of the address word to the capacitor-diode gates at least 10 microseconds earlier, and the PDP-4 at least 8 microseconds earlier, this condition is satisfied.

Each positive differentiated pulse is applied to the one input of its associated flip-flop (when the capacitor-diode gate is enabled), setting the flip-flop to its ONE state. Bit AC_0 in the

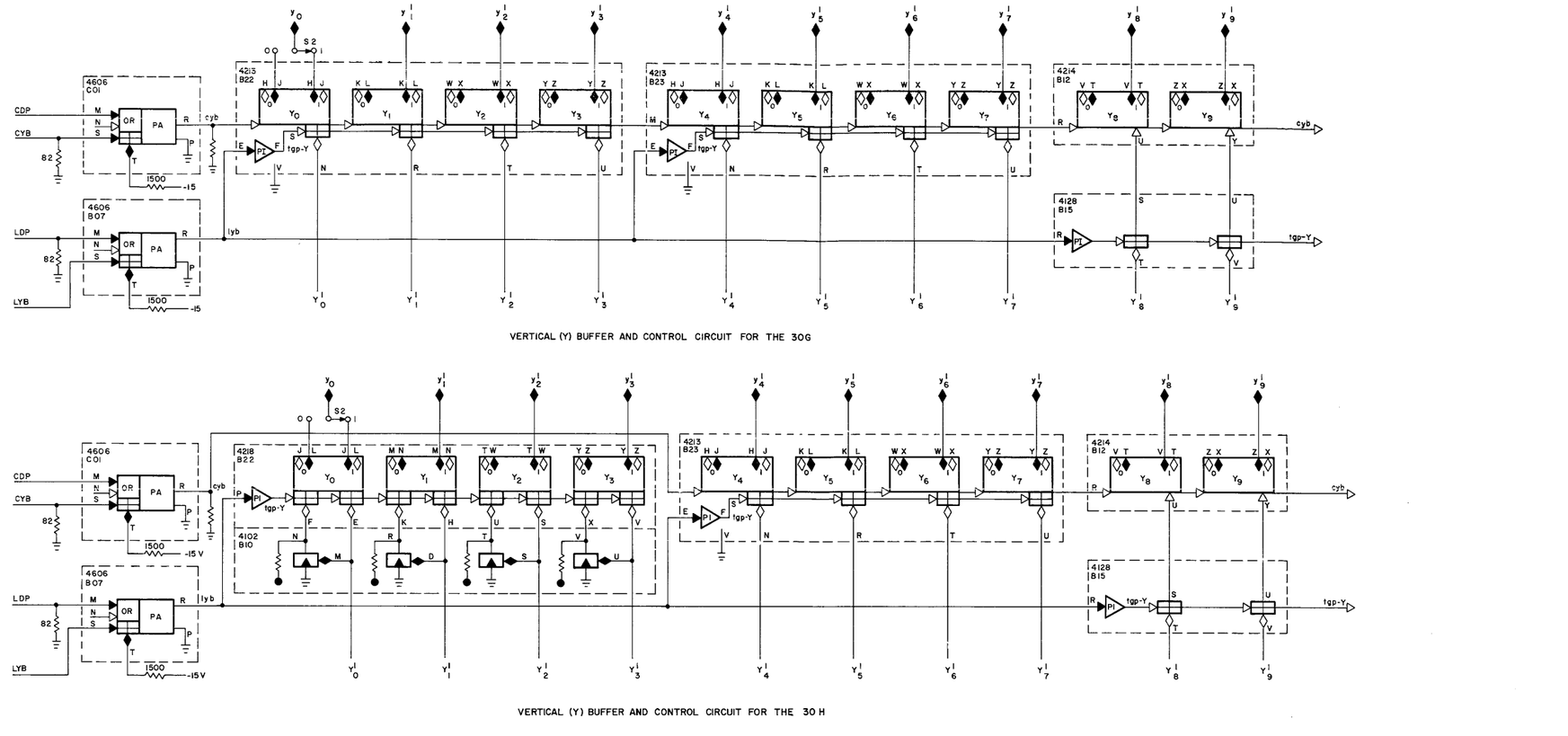


Figure 3-4 X Counter and Y Buffer Logic Block Diagram

PDP-1 and all AC bits from the PDP-4 are ground for the logic 1 state; so they are applied directly to the conditioning level inputs of the capacitor-diode gates. However, bits AC_{1-9} from the PDP-1 are -3 volts for the logic 1 state; so they are applied through inverters to the capacitor-diode gates. In this manner every bit of the X coordinate address word which is a logic 1 enables a gate, causing the associated flip-flop to be set to ONE, while every bit which is a logic O disables a gate, preventing the associated flip-flop from being changed from the ZERO state it already is in.

In order to avoid loading down the counter flip-flops, the output which is not connected to the complement input of the next more-significant flip-flop is used to control a level amplifier. Since these outputs are ground when the flip-flop holds a ONE and the level amplifier must receive a -3 volt input, inverters are used to effect the voltage change. The most-significant bit flip-flop does not require an inverter, and both of its outputs are applied to a double-throw switch. This enables the most-significant bit to be used either as a sign bit (center zero, X_0^0 = positive deflection, X_0^1 = negative deflection) or as part of the address word (offset zero, located on the left-hand edge).

The Y coordinate address word is loaded into the Y buffer in the same manner as the X coordinate was. The computer applies the bits of the Y coordinate address word directly to the conditioning level inputs of the capacitor-diode gates in the buffer in one memory cycle, and generates clear and load pulses during the next memory cycle(s). The PDP-4 uses separate clear and load pulses, CYB and LYB. Inverters are only necessary on the four more-significant inputs of the Type 30H because jam transferring is used. No inverters are necessary on the outputs. The outputs of the most-significant bit flip-flop are switched for offset zero (bottom edge) or center zero modes of operation.

The two less-significant bits of the Y coordinate word are applied to capacitor-diode gates in a separate Type 4128 module, which controls half of a Type 4214 Quadruple Flip-Flop module. The trigger pulse (tgp-y) from the pulse inverter in this module is ORed with the load x pulse (lxb) in the sequencer control circuit to initiate the point plotting cycle when enabled by the display command, DPY.

Intensity Level and Status Control Circuit

The intensity level and status control circuit is shown in Figure 3-5 for the Type 30G. The Type 30H is very similar, with only minor differences. This circuit contains the intensity buffer that selects and holds the intensity level of the displayed spot, and most of the circuits which supply signals to the computer indicating the status of the display.

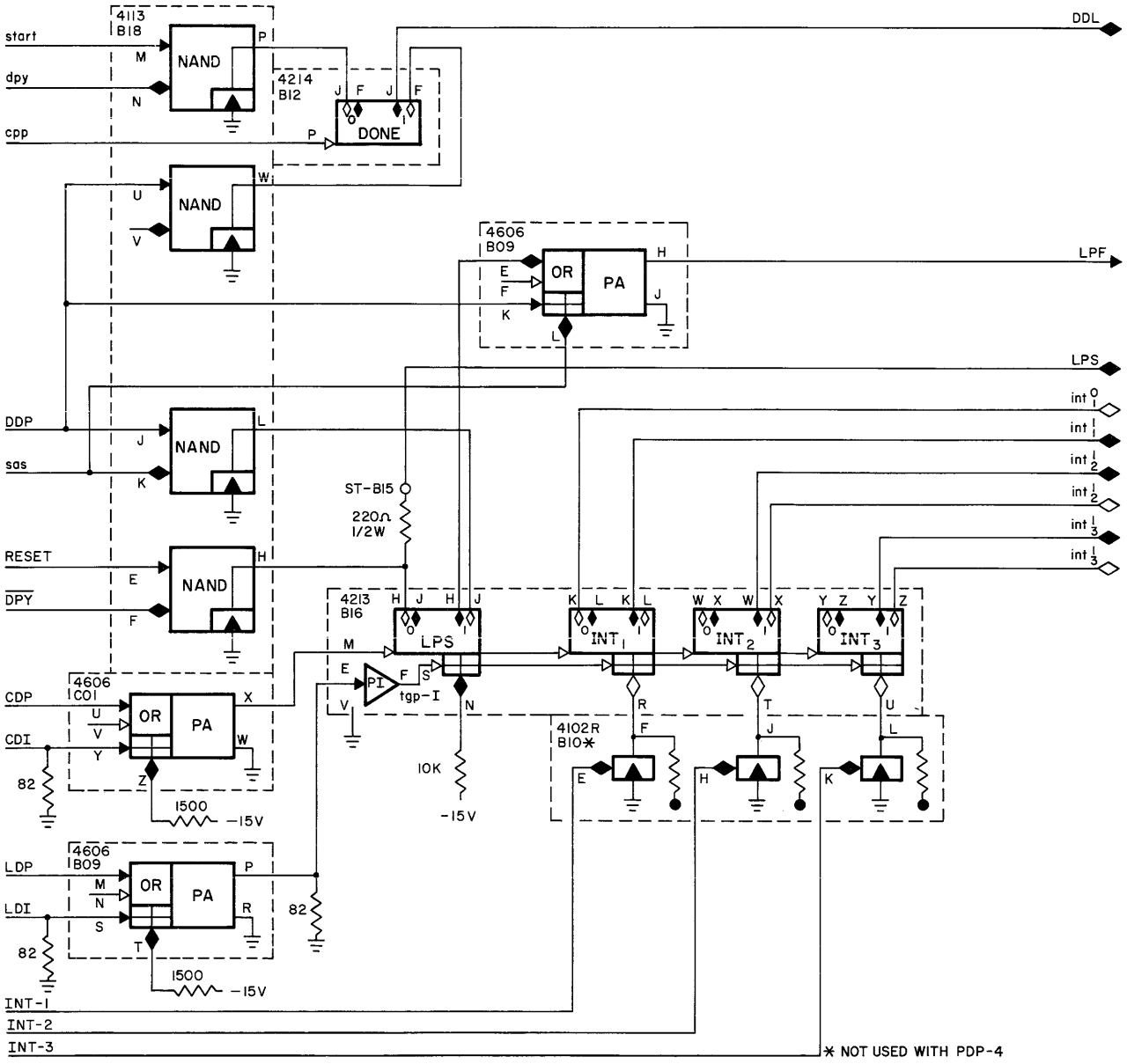


Figure 3-5 Intensity Level and Status Control Logic Block Diagram

Intensity Buffer - Eight different levels of intensity are possible with the Type 30G or the Type 30H. These levels correspond with the numerical value of a 3-bit 1's complement binary word supplied by the computer. The intensity buffer stores this word and generates appropriate control signals for the intensity bias circuit until the computer next clears the buffer.

When the PDP-1 is used, the 3-bit binary word which specified the intensity level is obtained from bits 9, 10, and 11 of the IOT instruction (MB_{9-11}). These are the INT-1, INT-2, and INT-3 signals, respectively. The IOT command which generates these signals also produces a

clear pulse (CDP) 1.1 microsecond later, and a load pulse (LDP) 3.3 microseconds later. The negative CDP pulse triggers a Type 4606 Pulse Amplifier, which produces a positive pulse that is applied to the direct clear inputs of the intensity buffer flip-flops and the light pen status flip-flop, setting them to their ZERO states. The negative load pulse (LDP) is also applied to a Type 4606 Pulse Amplifier, which produces a negative pulse that is applied to a pulse inverter in the buffer module. The pulse inverter produces a positive trigger gate pulse (tgp-I) that is applied to four capacitor-diode gates connected to the 1 inputs of the flip-flops.

The bits of the intensity word, which are -3 volts for logic 1, are inverted and applied to the conditioning level inputs of the intensity buffer's positive capacitor-diode gates. When these capacitor-diode gates are enabled by a ground potential on their conditioning level inputs for at least 3 microseconds, they differentiate the trigger pulse and set the associated flip-flop to its ONE state. In this manner the octal number specified by the three intensity bits is loaded into the buffer. Note that the capacitor-diode gate for the light pen status (LPS) flip-flop is permanently disabled by a negative potential on its conditioning level input.

The 3-bit intensity word from the PDP-4 is composed of AC bits 15, 16, and 17; therefore they must first be retrieved from memory and loaded into the AC before they can be transferred to the intensity buffer. The IOT command must also generate separate clear display intensity (CDI) and load display intensity (LDI) pulses at TP_5 and TP_7, respectively. The CDI and LDI pulses are applied to OR circuits in the same Type 4606 modules as the clear and load pulses from the PDP-1, so the operation is similar. However, the three inverters are not used because the AC bits are ground for logic 1.

TABLE 3-3 INTENSITY LOADING PROGRAM FOR PDP-4

Mnemonic Name	Code Number (octal)	Time (μsec)	Operation	Explanation
lac I	20iiii	16	C(iiii) ⇒ C(AC)	Intensity word in iiii loaded into AC
dlb	700706	8	C(AC) ⇒ C(IB)	Intensity buffer cleared at TP_5, intensity word transferred into buffer at TP_7.

The intensity buffer supplies a -3 volt signal for each bit to the indicators and to the computer when the bit is a logic 1. These are the —◆ int_1^1, —◆ int_2^1, and —◆ int_3^1 signals. It also supplies three signals to the intensity bias circuit, —◇ int_1^0, —◇ int_2^1, and —◇ int_3^1. Note that the two latter signals are the opposite outputs of the INT_2 and INT_3 flip-flops, while the former is the same as the INT_1 indicator signal. This reversal causes the output intensity level

to be offset from the octal number of the 3-bit intensity word, producing a normal intensity level that is slightly above the average level when the intensity buffer holds zero. The correlations between the intensity word, flip-flop states and outputs, and relative intensity levels are shown in Table 3-4.

TABLE 3-4 INTENSITY CORRELATIONS

Octal Number	Relative Intensity	Input Signal			Flip-Flop States			Output Signals		
		bit 1	bit 2	bit 3	bit 1	bit 2	bit 3	bit 1	bit 2	bit 3
4	0	+	0	0	1	O	O	-	-	-
5	1	+	0	+	1	O	1	-	-	0
6	2	+	+	0	1	1	O	-	0	-
7	3	+	+	+	1	1	1	-	0	0
0	4	0	0	0	O	O	O	0	-	-
1	5	0	0	+	O	O	1	0	-	0
2	6	0	+	0	O	1	O	0	0	-
3	7	0	+	+	O	1	1	0	0	0
	0 = dim 7 = bright	0 = ground + = +2.5 volts			O = logic O 1 = logic 1			0 = ground - = -3 volts		

Status Signals

Operating Status - The computer must know when any single point has been displayed, when the first half of the symbol word has been processed, and when the second half of the symbol word has been processed and the starting location of the next symbol incremented to the proper place. All this information is given by the display done pulse (DDP), a negative 0.4-microsecond pulse produced by the timing control circuit. The DDP pulse is also used to generate a display done level (DDL) that is used by the PDP-4.

The display done level (DDL) is produced by the done flip-flop in B12. This flip-flop is cleared to the ZERO state by the clear plot pulse (cpp) at the first clear or plot command from the computer, and by the start pulse at the beginning of the second half of the symbol generating process. The cpp pulse is produced by the sequencer control circuit and is applied to the direct clear input of the done flip-flop. The start pulse is ANDed with the negative display (DPY) enabling level by a NAND gate to produce a ground signal that is applied to the 1 output of the unbuffered done flip-flop. Both the start and dpy signals are generated by the timing control circuit.

Light Pen Status - When a light pen is being used to identify a particular display, the computer must know if and when the light pen sees the particular spot. If the light pen is looking at the

location of a spot when it is intensified, a negative saw a spot (sas) level will be produced by the light pen amplifier. The sas level will last longer than the 3 microsecond intensification period due to the persistency of the CRT's phosphor screen.

The sas level is ANDed with the DDP pulse to produce both light pen flag (LPF) and light pen status (LPS) signals for the computer. The LPF signal is a negative 0.4-microsecond pulse that is produced by a 4606 pulse amplifier in B09. This pulse amplifier is triggered by two methods. Normally the DDP pulse will trigger it if the sas level has been present at the conditioning level input of a capacitor-diode gate for approximately 1 microsecond. For the cases where this may not trigger the LPF pulse amplifier, the negative-going transition of the LPS signal is used.

The LPS signal is obtained from the LPS flip-flop. This flip-flop is initially cleared to the ZERO state by either the CDP or CDI (clear display intensity) pulse from the computer. In this state the LPS signal is grounded through 220 ohms. The sas signal and DDP pulse are applied to a negative NAND gate, temporarily grounding the output of the gate. This ground signal is applied to the 0 output of the unbuffered LPS flip-flop, setting it to the ONE state. In this state the LPS signal is clamped to -3 volts.

The LPS flip-flop can be reset to the ZERO state by a negative RESET pulse which is ANDed with the negative no display level ($\overline{\text{DPY}}$). These two signals are applied to a NAND gate which will temporarily ground the 1 output of the flip-flop, setting it to the ZERO state.

Format Determination

Most of the display format information must be loaded into the appropriate control flip-flops before the first half of the character word can be retrieved from memory. This information consists of the intensity, character size, normal or subscript location, automatic incrementing control, and automatic spacing control. The intensity has been described previously.

Subscript Control Circuit - The vertical location of the symbol matrix on a horizontal line can be one of two places as determined by the subscript control circuit. This consists of the subscript (sub) flip-flop in B11 and control circuits shown in Figure 3-6. The sub flip-flop is in the same module as the two less-significant bit flip-flops of the horizontal counter and is cleared by the cxb pulse. The capacitor-diode gate on its 1 input is permanently disabled by a negative voltage to prevent the tgp-x pulse from setting the flip-flop. The flip-flop is set and cleared instead by applying temporary ground signals on its outputs.

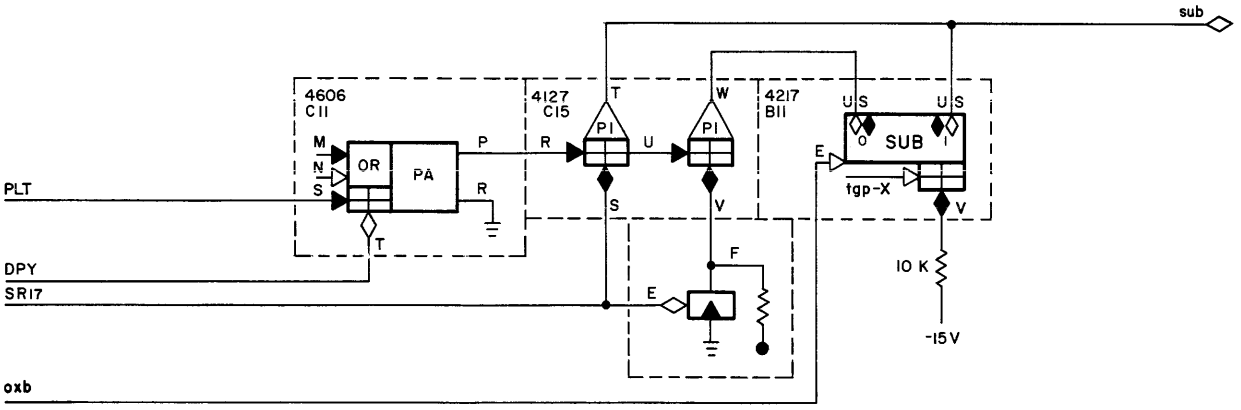


Figure 3-6 Subscript Logic Block Diagram

Bit SR_{17} of the first half of the character word determines the subscript location. This bit is applied directly to the conditioning level input of one capacitor-diode gate in C15 and is complemented by an inverter in C21 before being applied to the conditioning level input of another capacitor-diode gate in C15. The result is that only one of these capacitor-diode gates will be enabled at a time.

When the plot (PLT) pulse occurs, it triggers the pulse amplifier in C11 because the DPY signal had previously enabled a capacitor-diode gate there. (The PLT pulse must occur at least 1 microsecond after the DPY and SR_{17} levels.) The pulse amplifier produces a negative pulse that is applied to the trigger inputs of both capacitor-diode gates in C15. One of these is enabled, causing a ground pulse to be produced by its pulse inverter which sets flip-flop sub. The output of the flip-flop is the subscript (sub) signal, a ground level for the subscript position $\left(SR_{17}^{1}\right)$ and a -3 volt level for the normal position $\left(SR_{17}^{0}\right)$.

The symbol matrix is dropped into its subscript position by adding a subscript voltage, V_S, in superposition with the compensated vertical deflection voltage, V_V (see Figure 3-2). The V_S voltage is a function of the reference voltage, V_r, that determines the size of the symbol matrix. Both V_r and V_S are generated by the matrix size circuit, which is shown in Figure 3-7 along with part of the format control circuit. The symbol matrix therefore drops by some percentage of the matrix size as determined by the potentiometer on CB-C23.

Character Size - Four different matrix sizes are selected by bits SR_{16} and SR_{17}. Since these bits are used in both the vertical coordinate word and the two halves of the character word, they must be loaded into the format control buffer by a separate operation. These programs are shown in Tables 3-4 and 3-5. Note that the incrementing control bit, SR_{15}, is loaded at the same time.

TABLE 3-5 FORMAT LOADING PROGRAM FOR PDP-1

Mnemonic Name	Code Number (octal)	Time (μsec)	Operation	Explanation
lio F	22ffff	10	C(ffff) ⇒ C(I-O)	Format word in ffff loaded into I-O
glf	722026	10	C(I-O) ⇒ C(FB)	Format word transferred into format buffer

TABLE 3-6 FORMAT LOADING PROGRAM FOR PDP-4

Mnemonic Name	Code Number (octal)	Time (μsec)	Operation	Explanation
lac F	20ffff	16	C(ffff) ⇒ C(AC)	Format word in ffff loaded into AC
glf	701004	8	C(AC) ⇒ C(FB)	Format word transferred into format buffer

The format buffer consists of four unbuffered flip-flops in C20, each with positive capacitor-diode gates on their 0 and 1 inputs. A pulse inverter applies a positive trigger gate pulse (tgp-F) to each capacitor-diode gate when it receives a negative input pulse, setting the increment (incmt) and character size (CS_0 and CS_1) flip-flop to whichever state has been selected by the enabled capacitor-diode gate. (This method of transferring a word is called "jam transfer." It requires that one gate receive a bit and the other receive the complement of the bit.)

The 1 outputs of the CS flip-flops are applied to the base inputs of two level amplifier inverters in C24. When these inverters receive a ground input, they are cut off and their collectors are clamped at -10 volts. A -3 volt input saturates the inverters and their collectors go to ground. Each collector is connected to one input of a dc power amplifier in C25 through a weighed resistor. The other input of the dc power amplifier goes to a voltage divider on CB-C25 and is normally set for -6.25 volts. The difference of the fixed input and the selectable input, V_i, produces the reference voltage, V_r. The values of these voltages and the relationships between SR_{16} and SR_{17} and the matrix sizes are listed in Figure 3-7.

When a symbol matrix is in the normal position, sub is -3 volts and V_S is returned to ground through the potentiometer on CB-C23. When a symbol matrix is to be dropped to the subscript position, sub is ground and V_S is returned to the voltage V_r by the clamping diode.

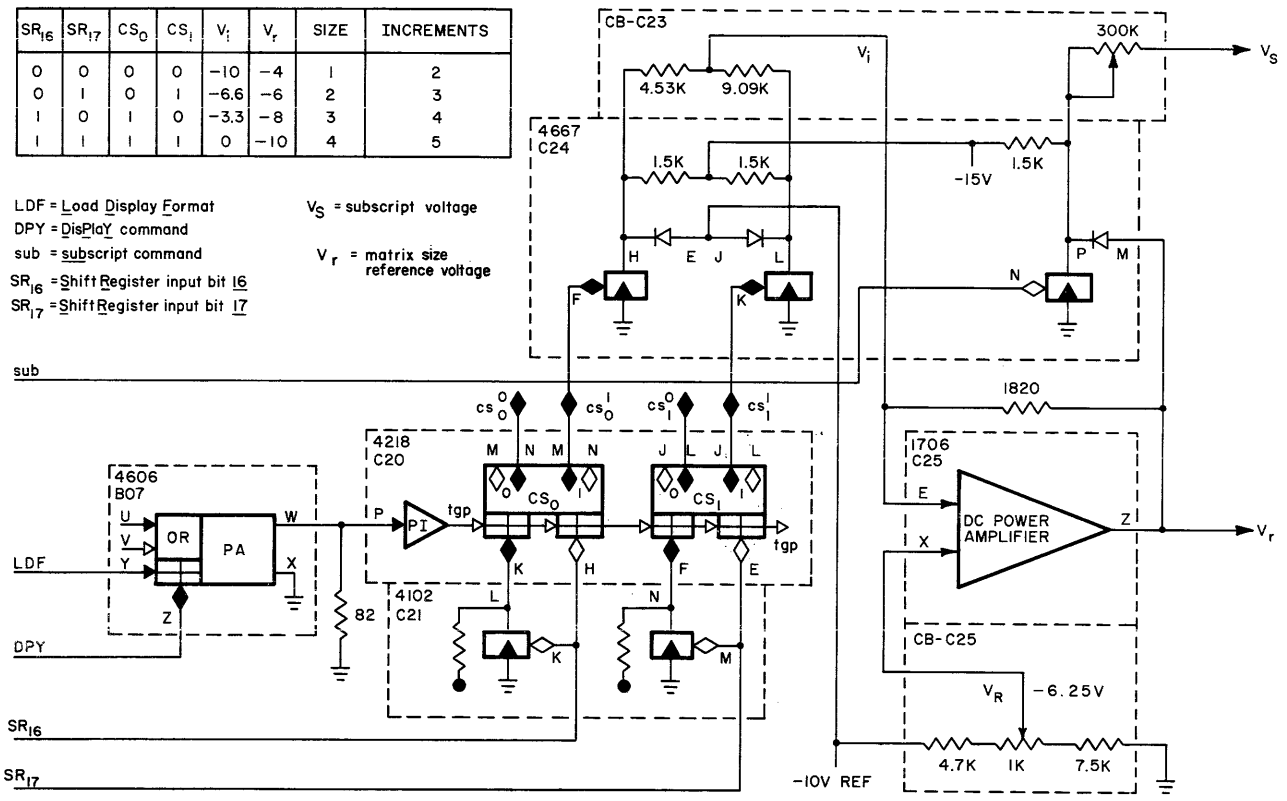


Figure 3-7 Character Size Logic Block Diagram

Incrementing and Spacing - When successive symbols are to be displayed on the same horizontal line, the Type 33 automatically moves the starting location of the next symbol matrix to the right. The next symbol can then be initiated by loading and displaying the first half of the character word, or the starting location can be moved one more position to the right without a display by a spacing command. This avoids the time required to retrieve words from memory and set up the deflection currents.

The starting position is moved by incrementing the X counter (see Figure 3-4). A number of increment X counter (inc-X) pulses are applied to a pulse amplifier in B09, which produces positive pulses that are applied to the complement input of the X_7 flip-flop. Each inc-X pulse adds four to the number held by the counter, moving the spot four places to the right. The inc-X pulses are produced by the matrix sequencer circuit after the old symbol has been displayed and before the DDP pulse occurs. The matrix sequencer circuit also determines the number of inc-X pulses, based on the character size.

The format control circuit contains both the incrementing (incmt) and spacing (space) flip-flops of the format buffer and the circuits that control these flip-flops. This portion of the format

control circuit is shown in Figure 3-8. The format loading command produces the disabling $\overline{DPY}$ level and a load format pulse (LDF). These are applied to a capacitor-diode gate in B07 which will trigger a pulse amplifier that produces a negative load pulse for the format buffer.

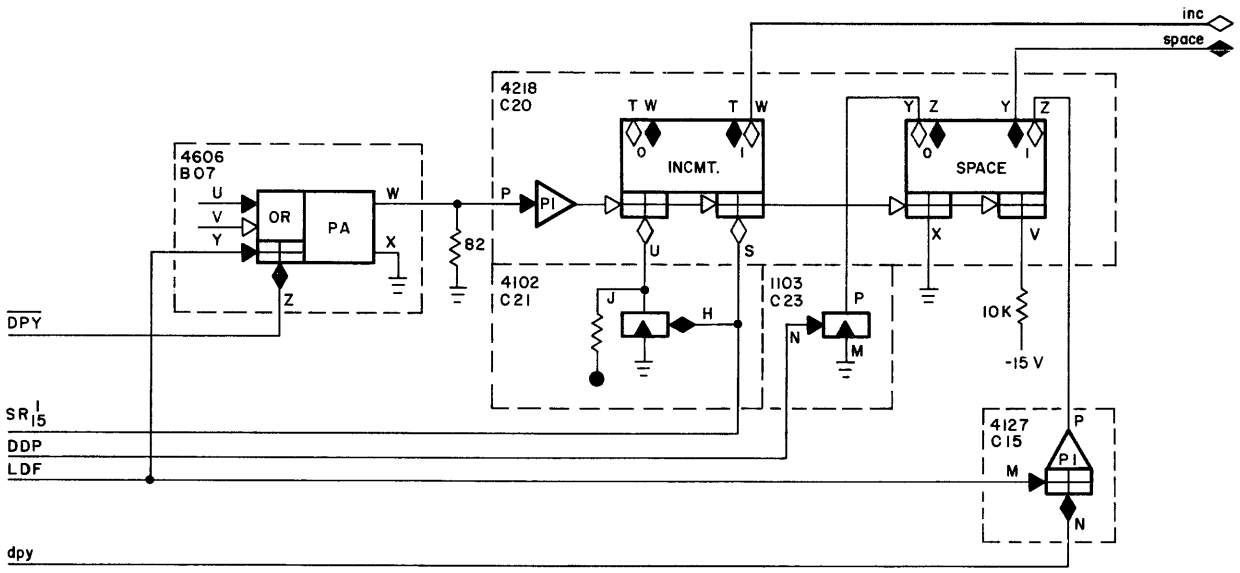


Figure 3-8 Increment and Space Control Logic Block Diagram

This load pulse is inverted and used to jam transfer SR_{15} into the incmt flip-flop and clear the space flip-flop. If SR_{15} is a 1, incmt will be set to the ONE state and enable the inc-X circuit of the matrix sequencer with a ground inc signal.

If the next display is not going to be adjacent to the previous symbol, SR_{15} is a O. This sets incmt to the ZERO state and makes inc -3 volts, disabling the inc-X circuit and enabling a gate which will stop the matrix plotting sequence after the last point is plotted.

In order to space the symbol matrix one character to the right, the incmt flip-flop must be set to ONE and then a separate space command must be issued. This is called gsp (720026 for PDP-1, 701044 for PDP-4). A counting sequence is then initiated which increments the X counter 4, 5, 6, or 7 times, depending on the size specified by the CS flip-flops. A DDP pulse is produced by the last incrementing pulse.

NOTE: The space command will transfer the contents of the I-O register (AC in the PDP-4) to the shift register and any ones in the seven more-significant bits will cause the spot to be intensified. The computer's register should be cleared before the space command occurs to avoid extra displays.

The space flip-flop is set by the LDF pulse when it triggers a capacitor-diode gate in C15 that has been enabled by the dpy level. The -3 volt space level turns on two inverters in the matrix sequencer circuit that enables the inc-X circuit and disables a count gate. The flip-flop is reset to the ZERO state by the DDP pulse, which produces a ground that is applied to the 1 output of the unbuffered flip-flop.

Symbol Matrix Generation

The symbol matrix is generated by the timing control circuit, sequencer control circuit, matrix sequencer, and the X- and Y-axis modifier circuits. It operates from a timing cycle that every 2 or 5 microseconds produces pulses which increment counters that control the X- and Y-axis modifier circuits in the order described by Figure 3-3. Additional control circuits select the proper number of incrementing pulses when incrementing or spacing, and produce the DDP pulse at the end of each operation.

Timing Control Circuit - The timing control circuit, Figure 3-9, controls the timing cycle, produces the start, shift, count, and done (DDP) pulses, and generates the intensify (int-A) and enable (dpy) levels. The selection of the point plotting or symbol generating modes is also made in this circuit.

A single point is displayed when the display enable level, DPY, enables the two point plotting capacitor-diode gates in B15 during the iot command that transfers a coordinate address word to the display. The load pulse produces a negative set X pulse and/or a positive tgp-Y pulse that triggers the enabled gate(s) and applies a positive signal to the deflection setup delay in B24. This initiates a 35-microsecond delay, producing a ground output from terminal U that is applied to a negative capacitor-diode gate in C15. (This gate is permanently enabled by a negative voltage on its conditioning level input.) The trailing edge of this signal triggers the gate when it goes back to -3 volts, producing a positive pulse from the pulse inverter. This signal is applied to the direct input of the intensify delay in B25, initiating a 3-microsecond intensify command (int-A) from terminal J that unblanks the CRT.

NOTE: When using the Type 370 Light Pen, the intensification delay can be reduced to 1.0 microsecond.

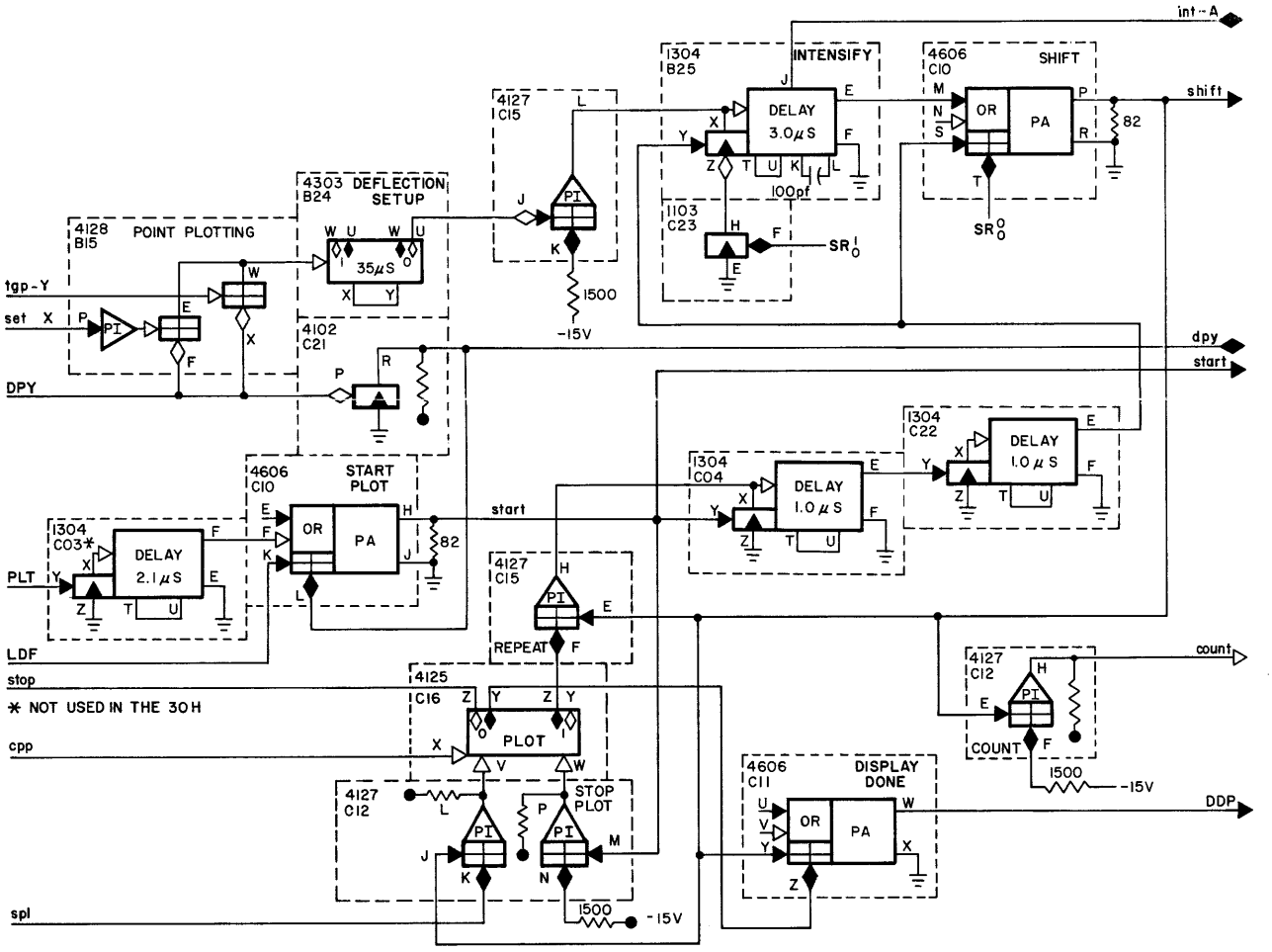


Figure 3-9 Timing Control Logic Block Diagram

At the end of the intensification delay a negative pulse is produced on terminal E that is applied to the direct input of the shift pulse amplifier in C10, producing a negative shift pulse that is applied to the capacitor-diode gate input of the display done pulse amplifier in C11. This gate is enabled by a -3 volt level from the plot flip-flop when in the point plotting mode; so the pulse amplifier is activated and produces the negative display done pulse (DDP). The plot flip-flop was initially set to the ZERO state by the clear plot pulse (cpp) from the sequencer control circuit.

The DPY level is also applied to an inverter in C21, producing the dpy signal. This is the complement of the DPY potential, and is used both for greater driving ability and for a -3 volt enabling level.

When a symbol is going to be displayed, the DPY level is -3 volts, disabling the point plotting gates in B15 and producing a ground dpy signal. The latter signal is applied to the conditioning

level input of a capacitor-diode gate in the start plot pulse amplifier in C10. This disables the gate and prevents the load format (LDF) pulse from activating the pulse amplifier. Therefore, when the format information is loaded into the buffer, the symbol plotting sequence is not started.

The symbol generating mode is initiated by the plot (PLT) command from the computer, a negative pulse occurring at TP_7 in the PDP-1 and at TP_1 in the PDP-4. In the 30H the PLT pulse is applied directly to the start plot pulse amplifier, while in the 30G it is delayed 2.1 microseconds by the 1304 delay module in C03. This delay is necessary in order to let the levels of the character word set up the read in capacitor-diode gates.

When the start plot pulse amplifier is activated, it produces a negative start pulse. This pulse reads the character word into the shift register, sets the plot flip-flop to ONE, and initiates the timing cycle by triggering a 1.0-microsecond delay.

The timing cycle starts with a 1.0-microsecond delay in C04. At the end of this time a negative pulse is produced that initiates a second 1.0-microsecond delay. This module, in turn, produces another negative pulse that is applied to two gates. One of these is a capacitor-diode gate in C10 that is enabled by the sr_0 flip-flop when it holds a ZERO. When this is the case, the gate triggers the shift pulse amplifier, producing a negative shift pulse. This in turn is applied to the trigger input of the repeat capacitor-diode gate in C15 which is enabled by the plot flip-flop (previously set to the ONE state). The repeat gate then produces a positive pulse that is applied to the direct input of the first delay to start the timing cycle all over again. The cycle stops when the plot flip-flop goes to ZERO and disables the repeat gate.

When the sr_0 flip-flop holds a ONE, the capacitor-diode gate in C10 is disabled and an inverter gate in B25 is enabled. The second 1.0-microsecond delay then triggers the 3.0-microsecond intensify delay. When the intensification time is over, the shift pulse amplifier is activated and the cycle continues as before.

The shift pulse is applied to the shift register, causing the register to shift the character word up one bit. Therefore each timing cycle examines the bit in sr_0, produces a 3-microsecond display if the bit is a 1, and shifts the word so that the next less-significant bit is moved into sr_0 for the next cycle to examine.

After the fifteenth bit of the first half of the character word is examined, the matrix sequencer circuit produces a -3 volt stop plot level (spl). This is applied to the conditioning level input of the stop plot capacitor-diode gate in C12, enabling the gate and causing the sixteenth shift pulse to set the plot flip-flop to ZERO. This disables the repeat capacitor-diode gate (after about 1 microsecond) and prevents the seventeenth shift pulse from continuing the

timing cycle. The plot flip-flop also enables the capacitor-diode gate in the display done module; so the seventeenth shift pulse produces a DDP pulse.

Each shift pulse also produces a count pulse from the permanently enabled count capacitor-diode gate in C12. The count pulse is applied to a 2-part counter in the matrix sequencer circuit where it causes the dot position of the symbol matrix to be moved according to the number held by the counter. See Figure 3-3 for the dot positions.

After the computer receives the DDP pulse, it transfers the second half of the character word to the display with a different iot command. This command produces the load format pulse (LDF) at TP_{10} in the PDP-1 and at TP_7 in the PDP-4, as well as the plot (PLT) pulse. Since the PLT pulse would clear the matrix sequencer counters, the display enable level (DPY) is used to prevent this. The DPY level produces an enabling dpy level for the start plot pulse amplifier, allowing the LDP pulse to bypass the PLT pulse in the 30G and start the second half of the symbol generating process. Operation in this half is the same as in the first half. When the last bit of the character word has been examined, the matrix sequence produces increment pulses to move the symbol matrix to the next starting location and then produces the spl signal to end the cycle.

Matrix Sequencer Circuit - This circuit keeps count of the number of timing cycles, generates appropriate control levels to change the deflection according to the count, and produces the stop, count of six, and stop plotting (spl) levels to properly end the two parts of the symbol generating mode. It also produces the correct number of incrementing (inc-X) pulses to move the starting location of the next symbol matrix to the right, based on the size of the matrix. Figure 3-10 shows the logic block diagram of the matrix sequencer circuit.

The basic component of the matrix sequencer circuit is a 2-part counter. This counter is divided into a section that counts to seven (for incrementing the spot up each vertical column of the matrix) and a section that counts to five (for spacing each column to the right).

The seven counter consists of three flip-flops in C16. The count pulses from the matrix sequencer circuit are applied to the complement input of the least significant bit flip-flop, 7_2, causing it to change its state each time. Every time a flip-flop changes from the ONE to the ZERO state, the transition of its 1 output from -3 volts to ground acts as a carry signal, which is applied to the complement input of the next more-significant bit flip-flop and causes it to change its state.

When the seven counter holds 6_8, the 7_0 and 7_1 flip-flops enable a transistor NAND gate, producing a -3 volt count-of-six level. The six signal in turn enables a capacitor-diode gate in the sequencer control circuit, causing the next shift pulse to produce the shift counter pulse (scp), and is also applied to one input of the incrementing size decoder in C19. The scp signal

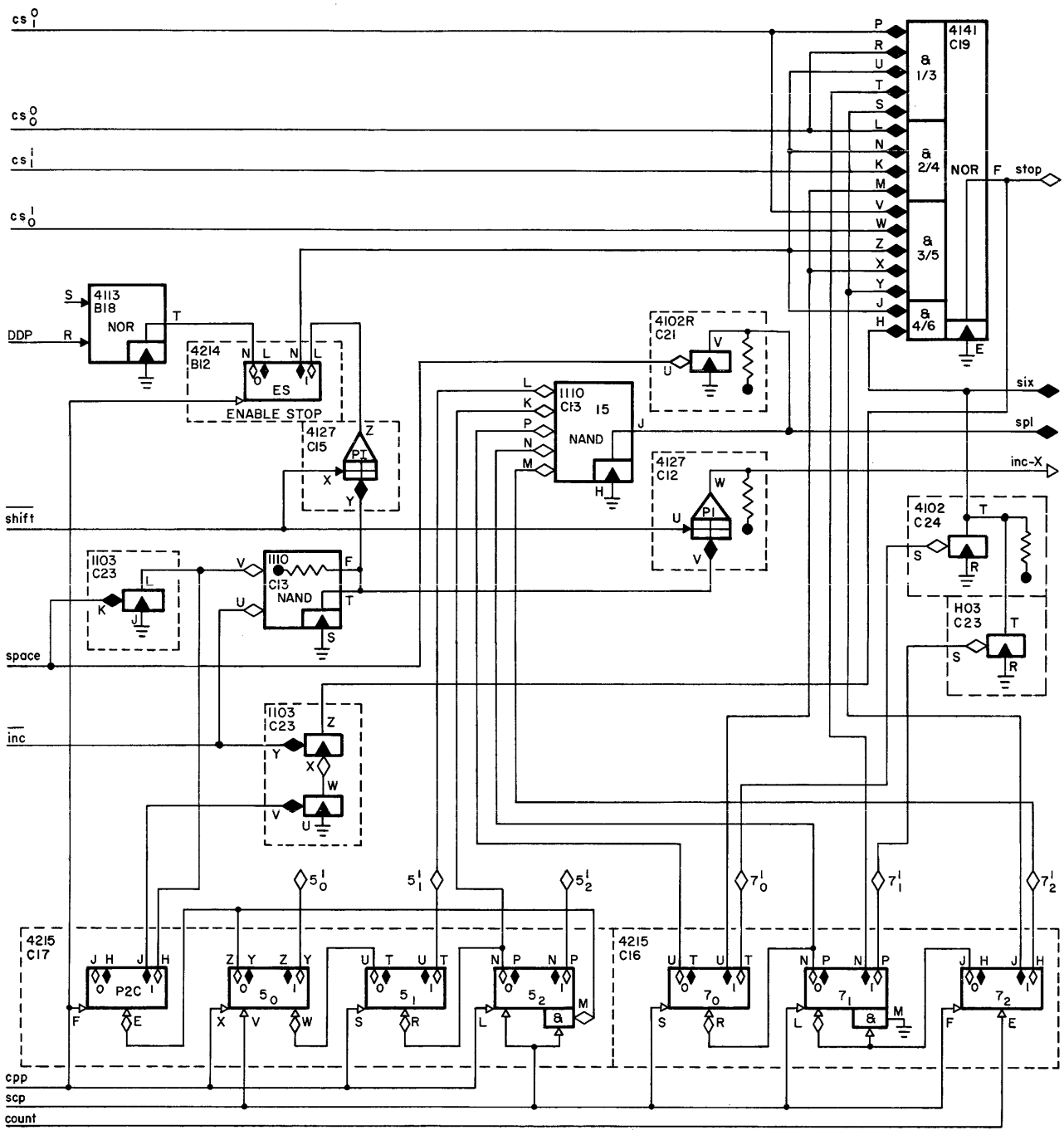


Figure 3-10 Matrix Sequencer Logic Block Diagram

is a positive 1-microsecond pulse that is applied to the seven counter as a clear pulse and to the five counter as a count-of-seven pulse. The seventh count pulse would set the seven counter to 7_8, but the scp pulse overrides it because of the 1.0 microsecond pulse width and resets the counter to 0_8.

The five counter consists of three flip-flops in C17. This counter is cleared, along with the plot two completed (P2C) and enable stop (ES) flip-flops by the clear plot pulse (cpp) from the sequencer control circuit. The cpp pulse occurs every time a coordinate address buffer is loaded at the start of each symbol generating cycle. Each scp pulse adds one to the counter on every seventh shift pulse until the counter holds 4_8. The next scp pulse (thirty-fifth shift pulse) resets the counter to 0_8 and sets the P2C flip-flop to the ONE state, indicating that the second half of the character word has been processed.

The 5_2 flip-flop has a single complement input that switches the flip-flop from either state to the opposite state when a positive pulse is applied as long as the AND gate is enabled by a ground level. This is supplied from the 1 output of the 5_2 flip-flop. However, when the AND gate has a -3 volt disabling level input, the complement input only switches the flip-flop from the ONE to the ZERO state. When the counter holds 4_8 (100), the 5_2 flip-flop disables the AND gate and the next scp pulse resets the counter.

After the fifteenth shift and count pulses have occurred, the seven counter holds 2_8 (010) and the five counter holds 1_8 (001). This number is detected by the 15 decoder in C13, a 5-input positive NAND gate, and its output inverter is cut off. The collector of this inverter shares a clamped load resistor with the collector of another inverter in C21. If this latter inverter is also cut off by a no space level ($\overline{\text{space}}$), then the output of the two ANDed circuits is the -3 volt stop plot level (spl). This signal enables the stop plot gate in the timing control circuit so that the sixteenth shift pulse will set the plot flip-flop to ZERO and halt the timing cycle (producing a DDP pulse) with the seventeenth shift pulse. (See Figure 3-9.)

When the computer starts the second half of the symbol generating cycle again, the first shift pulse that occurs is the eighteenth.

Operation continues until the thirty-fifth shift and count pulse occur and the P2C flip-flop is set to the ONE state. When this occurs, the 1 output of P2C applies an enabling -3 volt level to an inverter gate in C23 and the O output of P2C applies a ground input to a NAND gate in C13. If the increment (incmt) flip-flop has been set to the non-incrementing ZERO state, the inc signal is -3 volts. This turns on an enabled inverter in C23 which produces a ground stop level. The stop signal resets the plot flip-flop to the ZERO state and stops the symbol generating cycle when the thirty-sixth shift pulse occurs.

When the incmt flip-flop is set to the incrementing ONE state, inc is ground. This activates the NAND gate in C13 which produces an enabling -3 volt level for two capacitor-diode gates, one in C12 and one in C15. Each of these gates is then triggered by the thirty-sixth (and all succeeding) shift pulse and produces ground pulse outputs. The capacitor-diode gate in C12 produces the inc-X pulses that increment the X counter by four to move the starting

location of the next symbol matrix to the right. The capacitor-diode gate in C15 sets the enable stop (ES) flip-flop to the ONE state, producing a -3 volt enabling level that turns on the incrementing size decoder in C19. The ES flip-flop is reset to the ZERO state by the DDP pulse, as well as the cpp pulse.

The incrementing size decoder consists of four negative AND gates whose outputs are applied to a NOR gate that produces the ground stop level. Each AND gate receives a control level from the ES flip-flop and some other signal(s) that enables the gate when a predetermined number of inc-X pulses have occurred, based on the symbol matrix size. For example, if the character size buffers are set for size 1 (smallest), both cs_0^0 and cs_1^0 are -3 volts. The shift pulse that sets the ES flip-flop and produces the first incrementing pulse, inc-X_1, also produces a count pulse that adds one to the seven counter. After two more inc-X and count pulses occur, the counter holds 3_8, and the 7_1 and 7_2 flip-flops both apply -3 volt levels to the 1/3 AND gate. This enables the gate and produces the stop signal. However, one more inc-X and count pulse will be produced as well as the DDP pulse.

Both the 2/4 and 3/5 AND gates operate in a similar fashion. The 4/6 AND gate only receives the count-of-six signal because a smaller matrix size will decode some lesser count before six occurs.

Table 3-6 lists the steps and operations in a symbol generating cycle. The symbol word bit is that bit of each half of the character word that is examined before the shift and count pulse occurs. Note that the seven counter continues to count while incrementing after the character word has been displayed. STOP indicates that the incrementing size decoder is activated and produces the stop signal: one more inc-X and the DDP signals are produced by the next step.

When the symbol matrix location is to be spaced one character to the right without a display, a separate space command sets the space flip-flop to ONE and starts the symbol generating cycle with the equivalent of shift pulse thirty-six (see Table 3-6).

> NOTE: The seven most-significant bits in the computer's I-O (or AC) register must be zeros if no display is to occur.

The space signal is -3 volts when the space flip-flop is in the ONE state, saturating the transistor in C23 which sets the P2C flip-flop to the ONE state and enables the NAND gate in C13 (see Figure 3-10). Since the incmt flip-flop had previously been set to the ONE state, the inc signal is ground and the incrementing part of the cycle proceeds in the normal fashion. The cycle stops the same way as before, depending on the matrix size.

Sequencer Control Circuit - This circuit, shown in Figure 3-11, controls the symbol generating cycle. Whenever a coordinate address word is loaded into a buffer, a clx and/or a cyb pulse

TABLE 3-7 SYMBOL GENERATING CYCLE STEPS

Symbol Word Bit	Shift and Count Pulse Number	Matrix Counter States 5_0 5_1 5_2	Matrix Counter States 7_0 7_1 7_2	Other Actions and Operations
sr_0	1	0 0 0	0 0 1	PLT starts cycle
sr_1	2	0 0 0	0 1 0	
sr_2	3	0 0 0	0 1 1	
sr_3	4	0 0 0	1 0 0	
sr_4	5	0 0 0	1 0 1	
sr_5	6	0 0 0	1 1 0	six enabled
sr_6	7	0 0 1	0 0 0	scp generated
sr_7	8	0 0 1	0 0 1	
sr_8	9	0 0 1	0 1 0	
sr_9	10	0 0 1	0 1 1	
sr_{10}	11	0 0 1	1 0 0	
sr_{11}	12	0 0 1	1 0 1	
sr_{12}	13	0 0 1	1 1 0	six enabled
sr_{13}	14	0 1 0	0 0 0	scp generated
sr_{14}	15	0 1 0	0 0 1	spl enabled
sr_{15}	16	0 1 0	0 1 0	$\not 0 \rightarrow$ PLOT
sr_{16}	17	0 1 0	0 1 1	DDP generated, cycle halts
sr_0	18	0 1 0	1 0 0	PLT restarts cycle
sr_1	19	0 1 0	1 0 1	
sr_2	20	0 1 0	1 1 0	six enabled
sr_3	21	0 1 1	0 0 0	scp generated
sr_4	22	0 1 1	0 0 1	
sr_5	23	0 1 1	0 1 0	
sr_6	24	0 1 1	0 1 1	
sr_7	25	0 1 1	1 0 0	
sr_8	26	0 1 1	1 0 1	
sr_9	27	0 1 1	1 1 0	six enabled
sr_{10}	28	1 0 0	0 0 0	scp generated
sr_{11}	29	1 0 0	0 0 1	
sr_{12}	30	1 0 0	0 1 0	
sr_{13}	31	1 0 0	0 1 1	
sr_{14}	32	1 0 0	1 0 0	
sr_{15}	33	1 0 0	1 0 1	
sr_{16}	34	1 0 0	1 1 0	six enabled
sr_{17}	35	0 0 0	0 0 0	scp generated, $\not 1 \rightarrow$ P2C
——	36	0 0 0	0 0 1	inc X_1, $\not 1 \rightarrow$ ENABLE STOP
——	37	0 0 0	0 1 0	inc X_2
——	38	0 0 0	0 1 1	inc X_3, STOP: size 1
——	39	0 0 0	1 0 0	inc X_4, DDP generated, cycle ends: size 1 inc X_4, STOP: size 2
——	40	0 0 0	1 0 1	inc X_5, DDP generated, cycle ends: size 2 inc X_5, STOP: size 3
——	41	0 0 0	1 1 0	inc X_6, DDP generated, cycle ends: size 3 inc X_6, STOP: size 4
——	42	0 0 0	1 1 1	inc X_7, DDP generated, cycle ends: size 4

is generated and applied to an OR gate in C11. Either one of these pulses (or the PLT pulse when accompanied by a -3 volt no-display level, $\overline{DPY}$) will activate the associated pulse amplifier, producing a negative clear shift register (csr) pulse. The csr pulse is applied to three pulse amplifiers, one in the shift register and two in the sequencer control circuit. The latter two produce the clear plot pulse (cpp) and space count pulse (scp) signals. Both of these are applied to the matrix sequencer circuit and are discussed under that heading. The cpp pulse is also applied to the timing control circuit, shift register, and intensity level and status control circuit, see Figure 3-2.

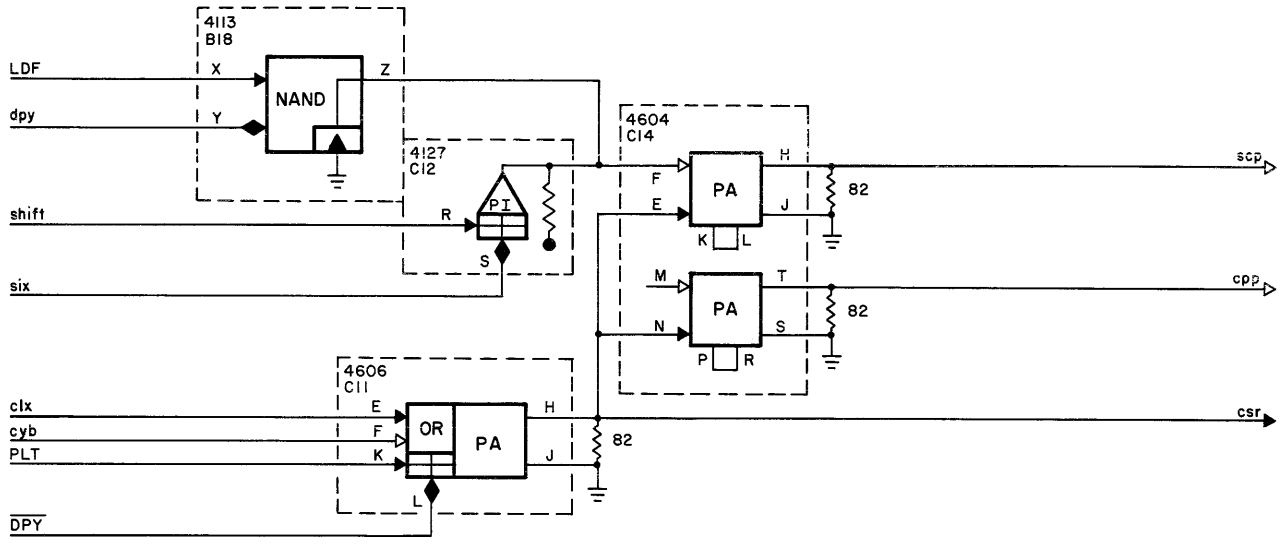


Figure 3-11 Sequencer Control Logic Block Diagram

The scp pulse is produced by two other pairs of signals. Whenever the seven counter holds 6_8, the six signal enables a capacitor-diode gate in C12, allowing the next shift pulse to trigger the gate, activating the pulse amplifier which produces the scp pulse. The scp pulse is also produced by the iot command that starts the second half of the symbol generating cycle. The display enable level, dpy, is ANDed with the LDF pulse by a NAND gate in B18 to activate the pulse amplifier that produces the scp pulse.

Deflection Modifier Circuits - These circuits consist of the X- and Y-axis modifiers, two identical 3-bit digital-to-analog converters with variable level amplifier gates shown in Figure 3-12. Each D-A converter changes the octal number held by the seven counter and five counter into the equivalent fraction of the common reference voltage, V_r. (Refer to the subscript control

circuit description and Figure 3-6 for an explanation of V_r.) When any flip-flop is in the ONE state the associated inverter is cut off and its collector goes to the V_r clamping level. The resistors of the D-A converters are weighed so that the resulting contributions to the output voltage are inversely proportional to their magnitude. The table in Figure 3-12 gives the relationships between the octal inputs (0 is -3 volts, 1 is ground) and the fractional values of V_r.

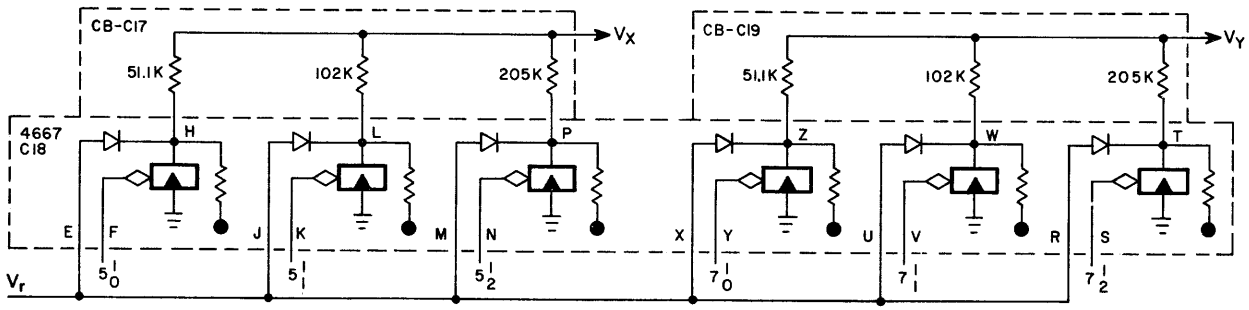


Figure 3-12 Deflection Modifier Logic Block Diagram

The two output voltages, V_X and V_Y, are applied to the reference inputs of the horizontal and vertical deflection amplifiers, respectively (see Figure 3-2). A change in the reference voltage is equivalent to a corresponding change in the opposite direction of the deflection voltage. The result is that as the counters increase their value, the V_X and V_Y voltages go more negative and the spot is deflected in a positive (up and right) direction.

Shift Register - This circuit consists of a pulse amplifier and five 4216 quadruple flip-flop modules. These flip-flops are manufactured with shifting connections between the input gates and the outputs, and with separate read-in gates. Figure 3-13 shows the logic block diagram of the shift register.

The register is cleared to zero by two pulses, the clear plot pulse (cpp) from the sequencer control circuit and a pulse produced by the pulse amplifier when the clear shift register (csr) pulse or the DDP pulse occurs. The two clear pulses are used because one pulse amplifier can only clear sixteen flip-flops. The csr and cpp pulses both occur whenever a coordinate loading command or the first plot command iot instruction occurs. The DDP pulse occurs after a single point is displayed or after each part of the symbol generating cycle is over, insuring that the register is cleared before the second half of the character word is applied.

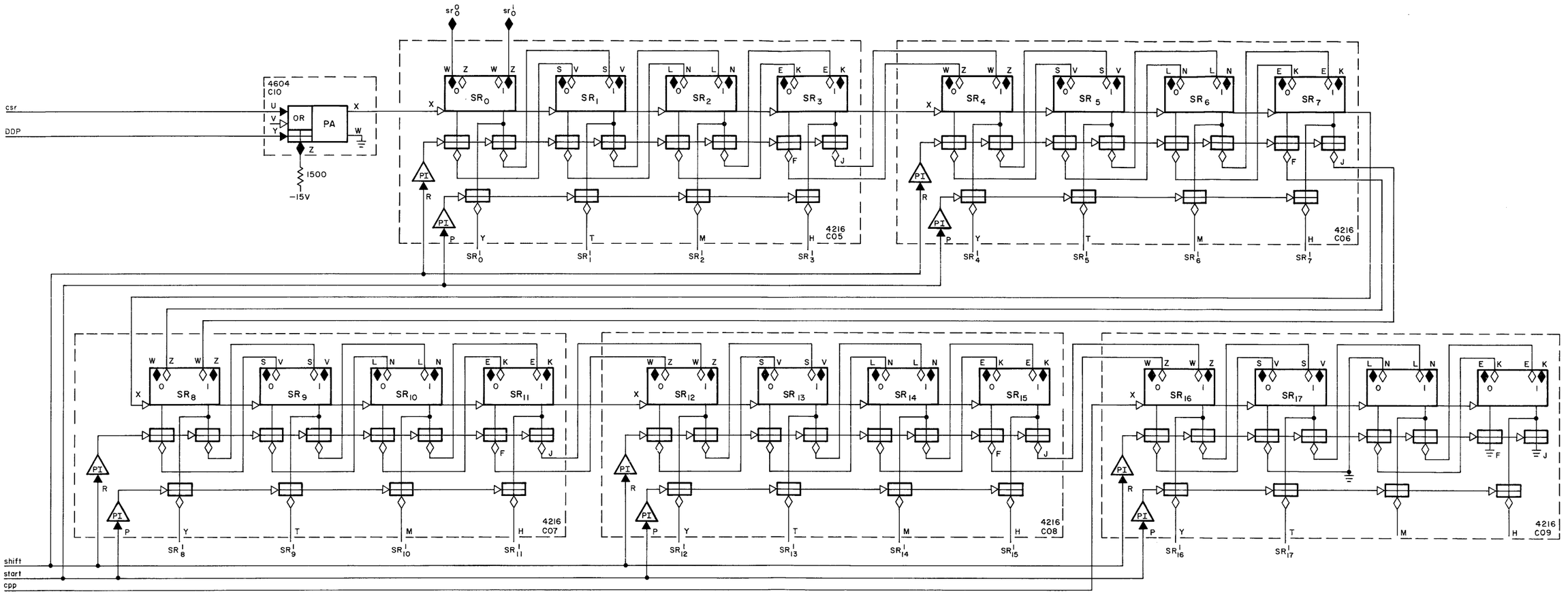


Figure 3-13 18-Bit Shift Register
Logic Block Diagram

Each time the iot instruction that transfers half of the character word occurs, the start pulse loads those bits of the word into the corresponding flip-flops. The SR bits are applied to the conditioning level inputs of positive capacitor-diode gates, and the start pulse is then applied to a pulse inverter in each module that triggers every gate that is enabled by a ground level (logic 1).

Every time a shift pulse occurs, the bit held by a flip-flop is transferred to the next more-significant flip-flop. The bit that was in SR_0 is lost, and the bit that goes into SR_{17} is always a O because the 0 input of this flip-flop is directly grounded. The shifting is accomplished by the jam transfer method.

SECTION 4

MAINTENANCE

Maintenance of the Type 30G or 30H display is the same as Section 4 of the Type 30E Precision CRT Display Manual, with the addition of the Maindec 30 Display Test procedures. MAINDEC 30 DISPLAY TEST manual, F-39-30, describes diagnostic test programs which should be run by the computer whenever any malfunctioning is suspected in either the Type 30 or 33, and approximately every six months as routine maintenance. The Type 33 requires no new tools or test equipment, assembly or disassembly procedures, or mechanical adjustments. Only the electrical adjustments listed in this section should require checking and adjusting.

ELECTRICAL ADJUSTMENTS

Delays

There are four delay periods in the Type 33 that may require adjustment. The method of adjusting these delays is the same as in the Type 30E manual.

Deflection Setup Delay - A 35-microsecond delay used in the point plotting mode to allow the current in the deflection coils to stabilize at the final value before the spot is intensified. The delay is provided by a 1304 multivibrator located in B24.

Intensification Delay - A 3.0-microsecond delay used to time the intensify command that unblanks the CRT. It is a 1304 multivibrator located in B25.

Character Setup Delay - A 2.1-microsecond delay used only in the Type 30G when a PDP-4 is operating the display. It compensates for the different memory cycle time when displaying successive characters on a line. It is provided by a 1304 multivibrator in C03.

Matrix Timing Delay - A 2.0-microsecond delay used in the symbol generating mode to time the steps of the symbol matrix sequence. It is composed of two 1.0-microsecond delays in series, located in C04 and C22. Each is a 1304 multivibrator. It is necessary to use two because of the recovery time of the 1304.

Character Size

The four character matrix sizes are controlled by the reference voltage V_r developed by a 1706 dc power amplifier in C25. These voltages may be varied by equal percentages by adjusting a potentiometer on CB-C25.

NOTE: When any character size adjustment is to be made, first adjust the raster size to 9-3/8 by 9-3/8 inches as detailed in the Type 30E Precision CRT Display Manual and the Maindec 30 Display Test. Be sure that the character size is at the largest selection by removing the 4218 module in C20.

Subscript Drop

The drop of any character into the subscript position is controlled by the voltage V_S. This may be adjusted by repeatedly displaying two symbol matrixes next to each other, with the latter in the subscript position, and adjusting the potentiometer on CB-C23 for the best location.

TROUBLESHOOTING

As in the Type 30E, it is only possible to troubleshoot the Type 33 when the logical operation is thoroughly understood. In general, the Maindec 30 Display Test programs should first be performed to be certain that the point plotting mode is operating normally. Then a simple program to repeatedly display a line of characters should be run and the flow of the various signals should be checked with an oscilloscope. If any circuit is found to be malfunctioning, investigate the inputs for proper voltage, correct timing, and normal shape.

Marginal Voltage Checking - The computer contains a separate Type 730 power supply which can be used for checking the operation of various circuits at marginal voltage limits. All circuits which are connected to the marginal voltage busses should operate normally at these voltages. If a circuit does not, it is an indication of deterioration that will ultimately lead to failure.

To check out the circuits in any row of modules, first turn on the 730 power supply and adjust it for the nominal voltage and polarity desired. Then throw the switch for that bus on the end of the row of modules down to the marginal position, and adjust the 730 to the marginal limits. Note at what voltage failure occurs and locate the failure.

Raising the bias voltage above +10 volts increases the transistor cutoff bias that must be overcome by the preceding state, causing low-gain transistors to fail. Lowering the bias voltage below +10 volts reduces the transistor base bias and noise rejection ratio and thus provides a test to detect high-leakage transistors and simulates high temperature operation. The normal working limits of individual modules are ± 5 volt variations of the bias supply.

Raising and lowering the -15 volt supply primarily increases and decreases the pulse outputs of pulse amplifiers only, since most collector load voltages are clamped at -3 volts. The normal working limits for individual modules is between -18 volts and -10 volts.

SECTION 5

DIAGRAMS

This section contains most of the information necessary to locate and identify the components and signal paths in the Type 33 Digital Symbol Generator, with either a Type 30G or Type 30H Precision CRT Display. The additional information is contained in the schematic diagrams of the modules and deflection amplifiers in the Type 30E Precision CRT Display manual.

The information in this section consists of cable and wiring schedules, and logic, wiring, and schematic diagrams. The proper diagrams and tables should be consulted for all signal tracing and troubleshooting operations. If any difficulty is experienced in reading a diagram, the equivalent DEC engineering drawing listed in Table 5-1 should be consulted.

TABLE 5-1 LIST OF DIAGRAMS

Figure	Title	Equivalent DEC No.
5-1	Type 30G Display Logic Diagram	BS-D-22403
5-2	Type 30G Symbol Generator Control Logic Diagram	BS-D-22403
5-3	Type 30G Symbol Generator Logic Diagram	BS-E-22403
5-4	Type 30G Logic Panel Wiring Diagram	WD-D-22404
5-5	Type 30H Display Logic Diagram	BS-D-54803
5-6	Type 30H Symbol Generator Control Logic Diagram	BS-E-54803
5-7	Type 30H Symbol Generator Logic Diagram	BS-D-54803
5-8	Type 30H Logic Panel Wiring Diagram	WD-D-54805
5-9	Type 30 Display Housing Diagram	CD-D-24406
5-10	Type 1103 Inverter Schematic	RS-1103
5-11	Type 1110 Diode Schematic	RS-1110
5-12	Type 1304 Delay Schematic	RS-1304
5-13	Type 1666 Analog Emitter Follower Schematic	RS-1666
5-14	Type 1706 Power DC Amplifier Schematic	RS-1706
5-15	Type 4102 Inverter Schematic	RS-4102
5-16	Type 4113 Diode Schematic	RS-4113
5-17	Type 4127 Capacitor-Diode-Inverter Schematic	RS-4127
5-18	Type 4128 Inverter-Capacitor-Diode Schematic	RS-4128
5-19	Type 4141 Diode Unit Schematic	RS-4141

TABLE 5-1 LIST OF DIAGRAMS (continued)

Figure	Title	Equivalent DEC No.
5-20	Type 4215 4-Bit Counter Schematic	RS-4215
5-21	Type 4216 Quadruple Flip-Flop Schematic	RS-4216
5-22	Type 4217 4-Bit Counter Schematic	RS-4217
5-23	Type 4218 Quadruple Flip-Flop Schematic	RS-4218
5-24	Type 4303 Integrating One-Shot Schematic	RS-4303
5-25	Type 4606 Pulse Amplifier Schematic	RS-4606
5-26	Type 4667 Level Amplifier Schematic	RS-4667

CABLE SCHEDULE

J-1 to Logic Panels in the Type 30G Interface Signals for PDP-4

Amphenol 115-115S

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
wht	1	C05Y	SR_0	wht	21	C07T	SR_9
wht	2	C05T	SR_1	wht	22	C07M	SR_{10}
wht	3	C05M	SR_2	wht	23	C07H	SR_{11}
wht	4	C05H	SR_3	wht	24	C08Y	SR_{12}
wht	5	C06Y	SR_4	wht	25	C08T	SR_{13}
wht	6	C06T	SR_5	wht	26	C08M	SR_{14}
wht	7	C06M	SR_6	wht	27	C08H	SR_{15}
wht	8	C06H	SR_7	wht	28	C09Y	SR_{16}
wht	9	C07Y	SR_8	wht	29	C09T	SR_{17}
wht	11	B12J	DDL	gry*	34	C01K	CXB
gry*	12	B18E	RESET	gry*	36	B07K	LXB
gry*	13	C01S	CYB	gry*	38	C11W	DDP
gry*	14	B07S	LYB	wht	45	ST-B15	LPS
gry*	15	C01Y	CDI	blu	47	+10 MC term	+10 MC
gry*	16	B09S	LDI	red	49	811-5	RTO
wht	17	B15F	DPY	blk	50	gnd	ground
gry*	19	C11K	PLT				
gry*	20	B07Y	LDF				

*twisted pair, blk is ground.

CABLE SCHEDULE (Continued)

J-1 to Logic Panels in the Type 30G
Interface Signals for the PDP-1

Amphenol
115-115S

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
wht	1	B01L	X_0	wht	29	C07Y	SR_8
wht	2	C02E	X_1	wht	30	C07T	SR_9
wht	3	C02H	X_2	wht	31	B10E	INT-1
wht	4	C02K	X_3	wht	32	B10H	INT-2
wht	5	C02M	X_4	wht	33	B10K	INT-3
wht	6	C02P	X_5	wht	34	C07M	SR_{10}
wht	7	C02S	X_6	gry*	35	C01E	CDP
wht	8	C02U	X_7	wht	36	C07H	SR_{11}
wht	9	C02W	X_8	gry*	37	B07E	LDP
wht	10	C02Y	X_9	gry*	38	C11W	DDP
gry*	16	B18E	RESET	wht	39	C08Y	SR_{12}
wht	17	B15F	DPY	gry*	40	B09H	LPF
gry*	19	C11K	PLT	wht	41	C08T	SR_{13}
gry*	20	B07Y	LDF	wht	42	C08M	SR_{14}
wht	21	C05Y	SR_0	wht	43	C08H	SR_{15}
wht	22	C05T	SR_1	wht	44	C09Y	SR_{16}
wht	23	C05M	SR_2	wht	45	ST-B15	LPS
wht	24	C05H	SR_3	wht	46	ST-B10	NAC
wht	25	C06Y	SR_4	blu	47	+10 MC term	+10 MC
wht	26	C06T	SR_5	wht	48	C09T	SR_{17}
wht	27	C06M	SR_6	red	49	811-5	RTO
wht	28	C06H	SR_7	blk	50	gnd	ground

*twisted pair, blk is ground.

CABLE SCHEDULE (continued)

J-1 to Logic Panels in the Type 30H
Interface signals for the PDP-1

Amphenol
115-115S

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
wht	1	B01L	X_0	wht	26	C06T	SR_5
wht	2	C02E	X_1	wht	27	C06M	SR_6
wht	3	C02H	X_2	wht	28	C06H	SR_7
wht	4	C02K	X_3	wht	29	C07Y	SR_8
wht	5	C02M	X_4	wht	30	C07T	SR_9
wht	6	C02P	X_5	wht	31	B10E	INT-1
wht	7	C02S	X_6	wht	32	B10H	INT-2
wht	8	C02U	X_7	wht	33	B10K	INT-3
wht	9	C02W	X_8	wht	34	C07M	SR_{10}
wht	10	C02Y	X_9	gry*	35	C01E	CDP
blu	11	B16K	INT_1	wht	36	C07H	SR_{11}
blu	12	B16W	INT_2	gry*	37	B07E	LDP
blu	13	B16Y	INT_3	gry*	38	C11W	DDP
gry*	14	C03T	INT-A	wht	39	C08Y	SR_{12}
	15	CRT housing	spare	gry*	40	B09H	LPF
gry*	16	B18E	RESET	wht	41	C08T	SR_{13}
wht	17	B15F	DPY	wht	42	C08M	SR_{14}
gry*	18	C11K	PLT	wht	43	C08H	SR_{15}
gry*	19	C10E	PLT	wht	44	C09Y	SR_{16}
gry*	20	B07Y	LDF	wht	45	ST-B15	LPS
wht	21	C05Y	SR_0	wht	46	ST-B10	NAC
wht	22	C05T	SR_1	blu	47	+10 MC term	+10 MC
wht	23	C05M	SR_2	wht	48	C09T	SR_{17}
wht	24	C05H	SR_3	red	49	811-5	RTO
wht	25	C06Y	SR_4	blk	50	and	ground

*twisted pair, blk is ground.

CABLE SCHEDULE (continued)

P-2 from Logic Panel B
Indicator Signals

Amphenol
143-022-04

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
w/blk	A	B01K	H-0	w/vio	J	B03V	H-7
w/brn	B	B03F	H-1	w/gry	K	B03X	H-8
w/red	C	B03J	H-2	w/blk	M	B03Z	H-9
w/orn	D	B03L	H-3	w/gry	W	J-1, 46	NAC
w/yel	E	B03N	H-4	w/blk	Y	-15 v	-15 volts
w/grn	F	B03R	H-5	w/brn	Z	gnd	ground
w/blu	H	B03T	H-6				

P-3 from Logic Panel B
Indicator Signals for the 30G

Amphenol
143-022-04

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
w/blk	A	B22H	V-0	w/gry	K	B12V	V-8
w/brn	B	B22K	V-1	w/blk	M	B12Z	V-9
w/red	C	B22W	V-2	w/grn	T	B16K	int_1
w/orn	D	B22Y	V-3	w/blu	U	B16W	int_2
w/yel	E	B23H	V-4	w/vio	V	B16Y	int_3
w/grn	F	B23K	V-5	w/gry	W	B16H	LPS
w/blu	H	B23W	V-6	w/blk	Y	-15 v	-15 volts
w/vio	J	B23Y	V-7	w/brn	Z	gnd	ground

CABLE SCHEDULE (continued)

P-3 from Logic Panel B
Indicator Signals for the 30H

Amphenol
143-022-04

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
w/blk	A	B22J	V-0	w/gry	K	B12V	V-8
w/brn	B	B22K	V-1	w/blk	M	B12Z	V-9
w/red	C	B22T	V-2	w/grn	T	B16K	int_1
w/orn	D	B22Y	V-3	w/blu	U	B16W	int_2
w/yel	E	B23H	V-4	w/vio	V	B16Y	int_3
w/grn	F	B23K	V-5	w/gry	W	B16H	LPS
w/blu	H	B23W	V-6	w/blk	Y	-15 v	-15 volts
w/vio	J	B23Y	V-7	w/brn	Z	gnd	ground

J-4 from Logic Panel A
Deflection Signals for the 30G

Amphenol
126-198

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
coax	A	A08B	left	coax	D	A17B	down
coax	B	A08A	right	coax	E	A17A	up
w/vio	C	+10 v	+10 volts	blu	F	+50 v	+50 volts
				blk	H	gnd	ground

J-4 from Logic Panel A
Deflection Signals for the 30H

Amphenol
126-198

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
coax	A	A08B	left	coax	D	A17B	down
coax	B	A08A	right	coax	E	A17A	up
orn	C	+10 v	+10 volts	blu	F	+50 v	+50 volts
				blk	H	gnd	ground

CABLE SCHEDULE (continued)

P-4 from Component Mounting Plate
Deflection Signals

Amphenol
126-195

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
coax	A	J-6, 6	left	coax	D	J-6, 8	down
coax	B	J-6, 7	right	coax	E	J-6, 5	up
w/orn	C	ST-SPU	+10 volts	red	F	J-6, 1	+50 volts
				blk	H	gnd	ground

J-5 from Logic Panel B
Intensity and Light Pen Signals for the 30G

Amphenol
126-221

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
w/brn	B	B16K	int_1	w/grn	F	J-1, 14	INT-A
w/red	C	B16X	int_2	w/blu	H	B18K	sas
w/orn	D	B16Z	int_3	orn	J	-15 v	-15 volts
w/yel	E	B25J	int-A	w/gry	K	gnd	ground

J-5 from Logic Panel B
Intensity and Light Pen Signals for the 30H

Amphenol
126-221

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
w/brn	B	B16K	int_1	w/grn	F		
w/red	C	B16X	int_2	w/blu	H	B18K	sas
w/orn	D	B16Z	int_3	w/vio	J	-15 v	-15 volts
w/yel	E	B25J	int-A	w/gry	K	gnd	ground

CABLE SCHEDULE (continued)

P-5 from SPU Container
CRT Control Signals

Amphenol
126-221

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
w/brn	B	D03J	int_1	w/grn	F	D03R	INT-A
w/red	C	D03U	int_2	w/blu	H	D01H	sas
w/orn	D	D03X	int_3	w/vio	J	D01C	-15 volts
w/yel	E	D03P	int-A	w/gry	K	D01D	ground

J-6 from Component Mounting Plate
Deflection Currents to Yoke

Cinch-Jones
S-308-FP

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
red	1	P-4, F	+50 volts	pink	5	R4, ct	up
red	2	R3	+50 volts	yel	6	R5, ct	left
red	3	D02E	+50 volts	orn	7	R6, ct	right
red	4	C3, +	+50 volts	brn	8	R3, ct	down

P-6 from Deflection Yoke
Deflection Currents

Cinch-Jones
S-308-FH

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
blu	1	no id.	+50 volts	red	5	no id.	up
grn	2	no id.	+50 volts	orn	6	no id.	left
blk	3	no id.	+50 volts	yel	8	no id.	right
wht	4	no id.	+50 volts	brn	8	no id.	down

CABLE SCHEDULE (continued)

J-7 from Component Mounting Plate
Focus Current

Cinch-Jones
S-302-AB

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
blk	1	gnd lug	ground	yel	2	T1, col.	focus

P-7 from Focus Coil
Focus Current

Cinch-Jones
P-302-CCT

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
grn	1	no id.	ground	yel	2	no id.	focus

J-8 from Type 770 Power Supply
CRT Bias and Heater Power

Amphenol
26-4404-8S

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
red	1	770-1	+250 v	blu	5	770-5	-150 volts
blk	3	770-3	ground				
wht	4	770-4	6.3 vac	blk	8	770-8	6.3 vac

P-8 from Component Mounting Plate
CRT Bias and Heater Power

Amphenol
26-4404-8P

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
grn	1	D02U	+250 volts	blu	5	D02V	-150 volts
blk	3	gnd	ground				
w/brn	4	ST-H1	6.3 vac	w/brn	8	ST-H3	6.3 vac

J-9 from Type 770 Power Supply
CRT Ultor Voltage

Winchester
456

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
wht	A	770-A	+10kv	blk	B	770-B	ground

P-9 from CRT Tube
CRT Ultor Voltage

Winchester
456

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
wht	A	anode cap	+10kv	shield	B	none	ground

S-10 from CRT Housing
CRT Socket Connections

12-pin Tube Socket

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
brn	1	ST-H1	6.3 vac	orn	10	D02T	+200 v
grn	2	D02X	bias	yel	11	D02Y	INT
				brn	12	ST-H2	6.3 vac

P-11 from Power End Panels
+10 and -15 volt Logic Power

Cinch-Jones
P-308-FHT

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
grn	1 and 2	+10 v	+10volts	blk	7 and 8	gnd	ground
red	3 and 4	-15 v	-15volts				

J-12 from C03J
X Analog Voltage

BNC
Microdot 50-3920

J-13 from C03F
Y Analog Voltage

BNC
Microdot 50-3920

J-14 from C03S
Z Intensifying Command

BNC
Microdot 50-3920

P-16 to 811 Power Control Panel
Primary 115 Volt 60 CPS Power

Miller Electric
034-2

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
blk	1	FL1	115vac	grn	3	chassis	ground
wht	2	FL2	115vac				

P-17 from NJE Power Supply
Main AC Power

Amphenol
160-5

Wire Color	Connector Terminal	Equipment Connection	Line Name	Wire Color	Connector Terminal	Equipment Connection	Line Name
blk	1	tb 1-1	115vac	grn	3	chassis	ground
wht	2	tb 1-2	115vac				

P-18 to J-19
115 Volt 60 CPS Power for Type 770 Power Supply

Amphenol
160-5 and 160-4

P-20 from 811 Power Control Panel
115 Volt 60 CPS Power for Power Supplies

Amphenol
160-5

J-21 from C03N
Horizontal Reference Voltage

BNC
Microdot 50-3920

J-22 from C03L
Vertical Reference Voltage

BNC
Microdot 50-3920

J-23 from C03T
Positive Intensifying Command

BNC
Microdot 50-3920

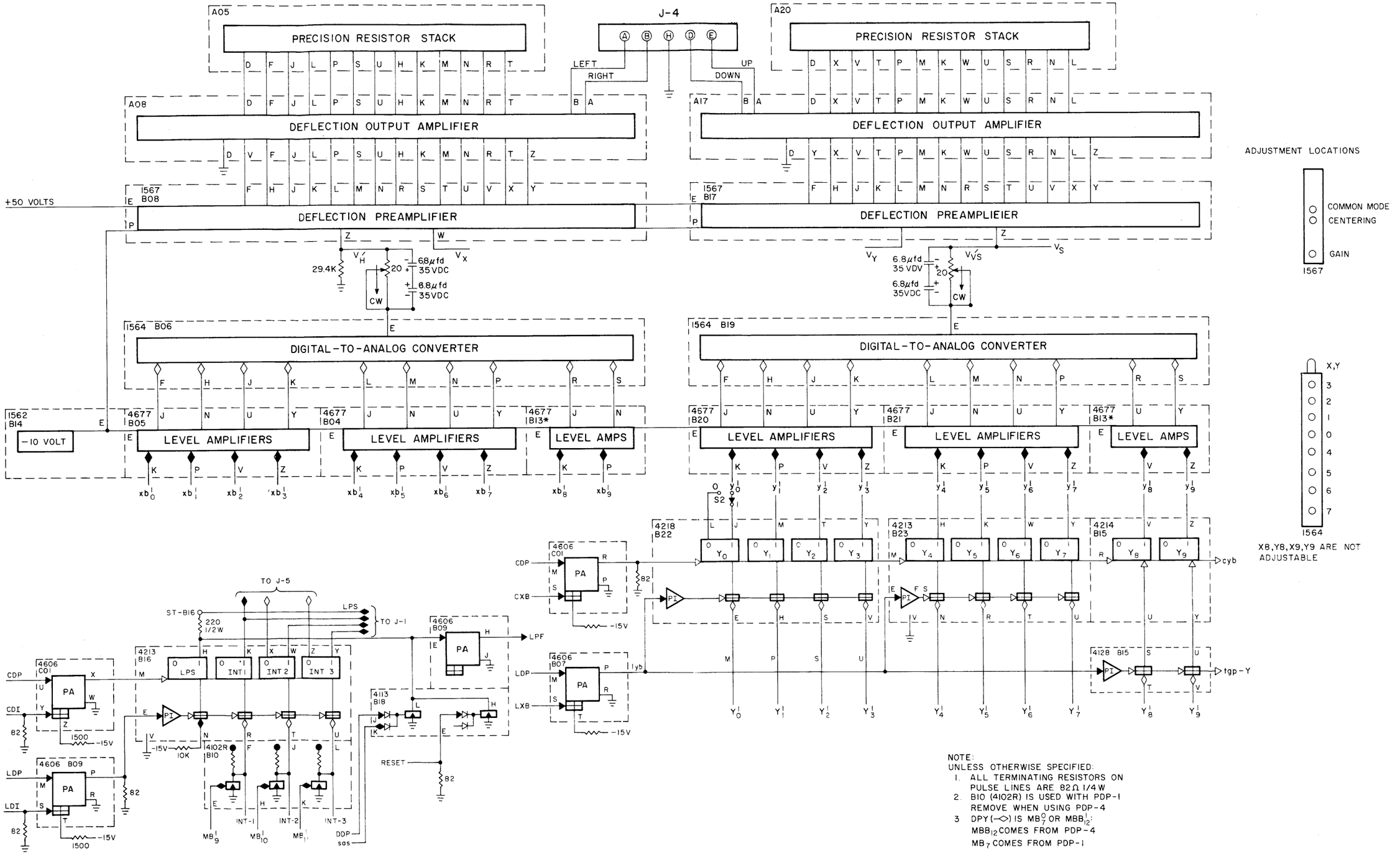
WIRING SCHEDULE

Wire Color	From	To
wht	811-2	811-8
wht	811-3	811-6
blk	811-6	cooling fans
blk	811-8	sail switch
brn	811-9	sail switch
red	811-10	cooling fans
blk	EQR 60-6B, tb 1-1	P-11, 1
wht	EQR 60-6B, tb 1-2	P-11, 2
jumper	EQR 60-6B, tb 1-3	EQR 60-6B, tb 1-4
jumper	EQR 60-6B, tb 1-4	EQR 60-6B, tb 1-3
jumper	EQR 60-6B, tb 1-5	EQR 60-6B, tb 1-6
jumper	EQR 60-6B, tb 1-6	EQR 60-6B, tb 1-5
jumper	EQR 60-6B, tb 1-7	EQR 60-6B, tb 1-8
jumper	EQR 60-6B, tb 1-8	EQR 60-6B, tb 1-9
jumper	EQR 60-6B, tb 1-9	EQR 60-6B, tb 1-8
jumper	EQR 60-6B, tb 1-10	EQR 60-6B, tb 1-11
jumper	EQR 60-6B, tb 1-11	EQR 60-6B, tb 1-12
grn	EQR 60-6B, tb 1-12	P-11, 3; chassis gnd
red	EQR 60-6B 50 v pos.	+50 v standoff on deflection amp.
blk	EQR 60-6B 50 v neg.	gnd on deflection amp. panel

30G Internal Wiring for use with PDP-4

Wire Color - White

From	Name	To	Name	To	Name	To	Name
C07Y	SR_8	B01L	X_0	B22N	Y_0		
C07T	SR_9	B01R	X_1	B22R	Y_1		
C07M	SR_{10}	B01V	X_2	B22T	Y_2		
C07H	SR_{11}	B01Z	X_3	B22U	Y_3		
C08Y	SR_{12}	B02L	X_4	B23N	Y_4		
C08T	SR_{13}	B02R	X_5	B23R	Y_5		
C08M	SR_{14}	B02V	X_6	B23T	Y_6		
C08H	SR_{15}	B02Z	X_7	B23U	Y_7	B16R	INT-1
C09Y	SR_{16}	B11L	X_8	B15T	Y_8	B16T	INT-2
C09T	SR_{17}	B11R	X_9	B15V	Y_9	B16U	INT-3



ADJUSTMENT LOCATIONS

X8,Y8,X9,Y9 ARE NOT ADJUSTABLE

NOTE:
UNLESS OTHERWISE SPECIFIED:
1. ALL TERMINATING RESISTORS ON PULSE LINES ARE 82Ω 1/4 W
2. B10 (4102R) IS USED WITH PDP-1 REMOVE WHEN USING PDP-4
3. DPY (<>) IS MB_7^0 OR MBB_{12}^1:
   MBB_{12} COMES FROM PDP-4
   MB_7 COMES FROM PDP-1

Figure 5-1 Type 30G Display Logic Diagram

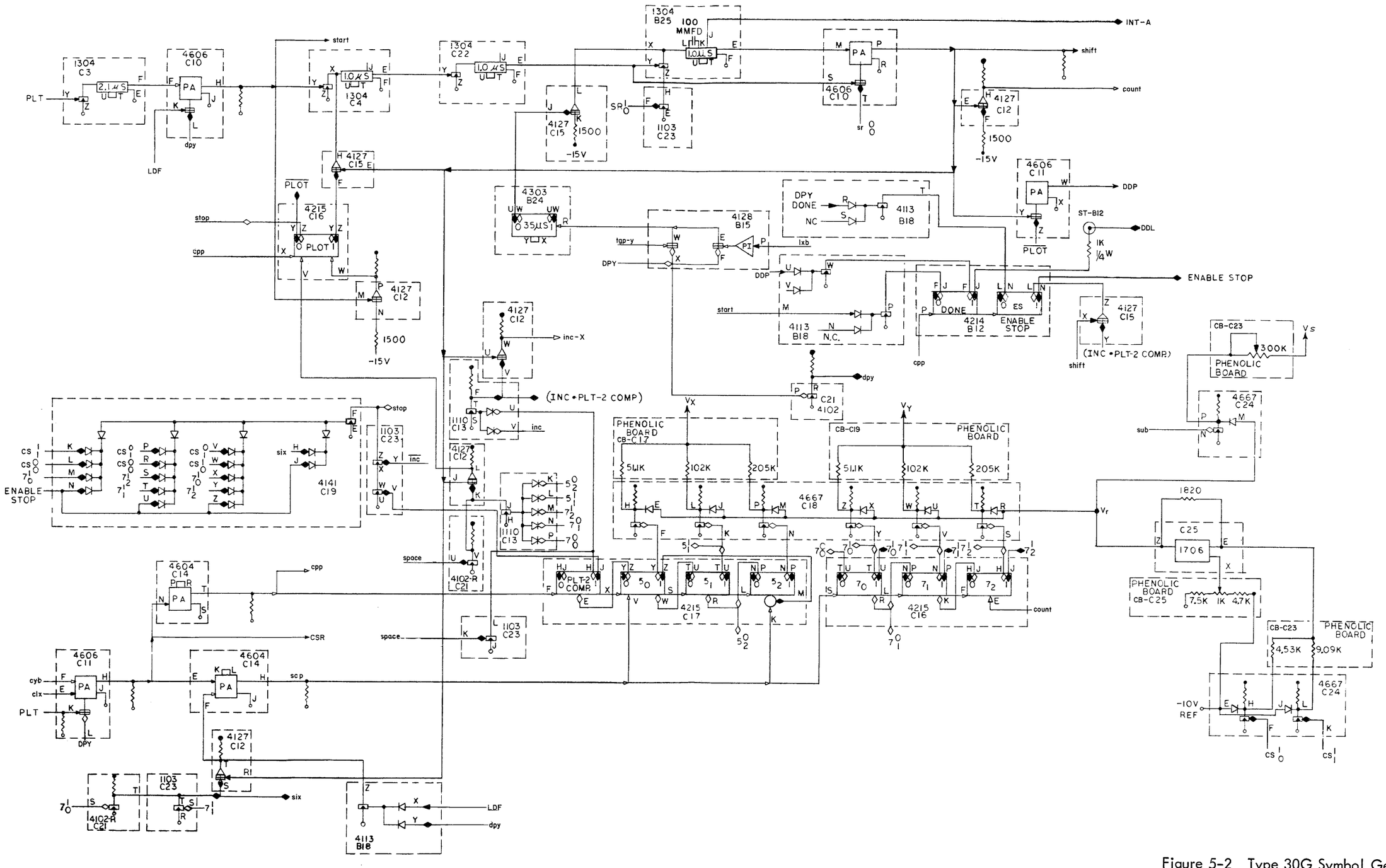


Figure 5-2 Type 30G Symbol Generator Control Logic Diagram

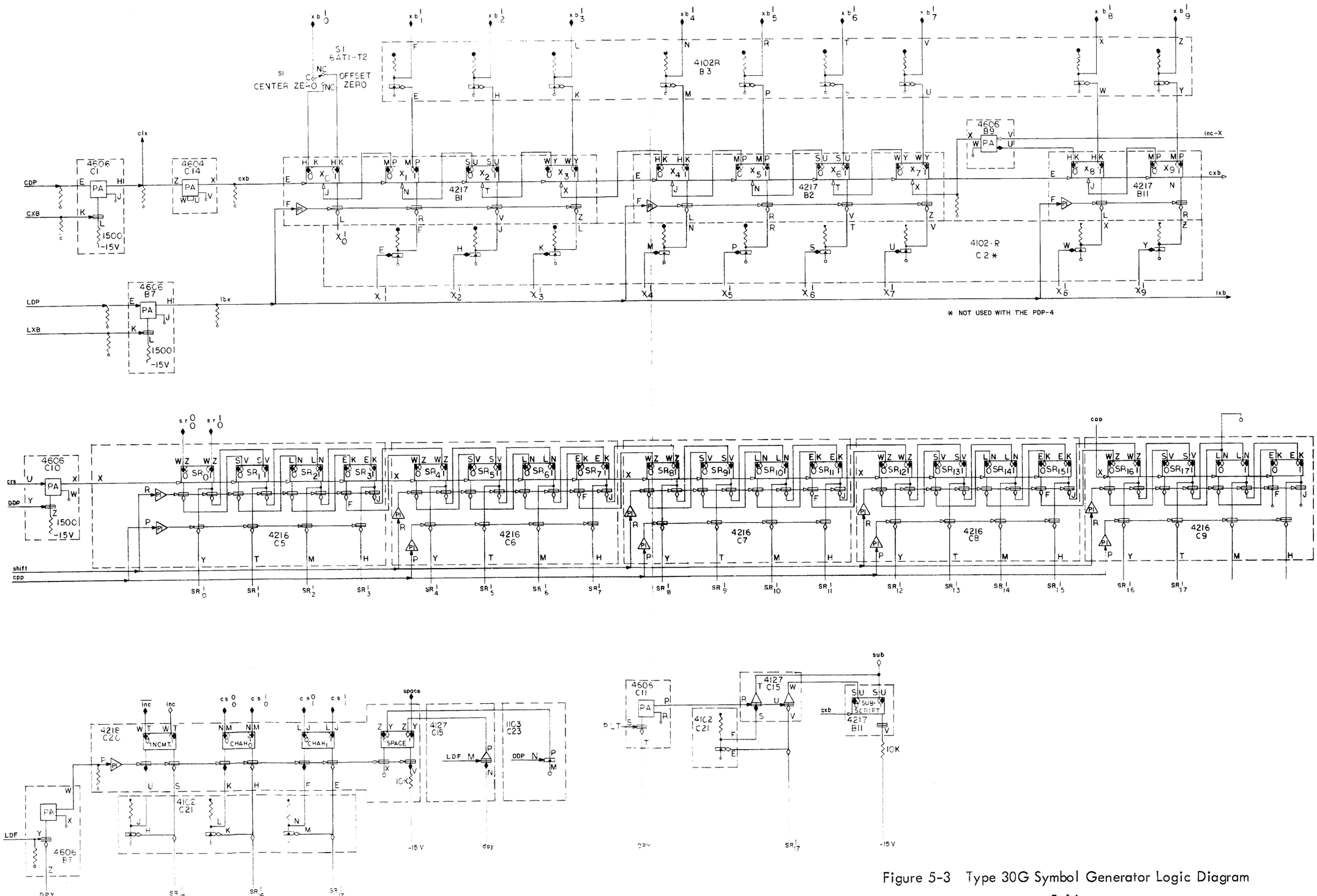


Figure 5-3 Type 30G Symbol Generator Logic Diagram

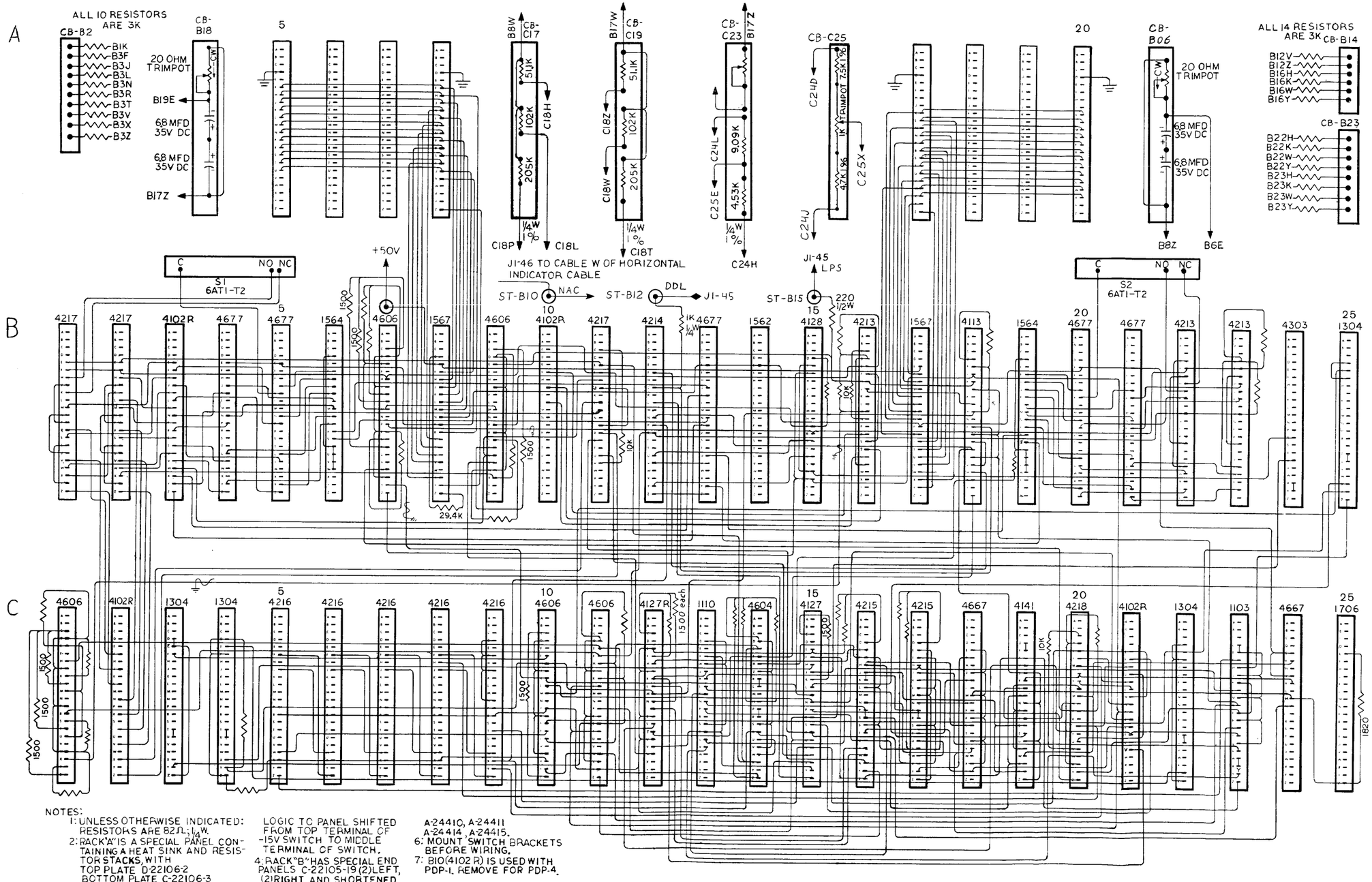


Figure 5-4 Type 30G Logic Panel Wiring Diagram

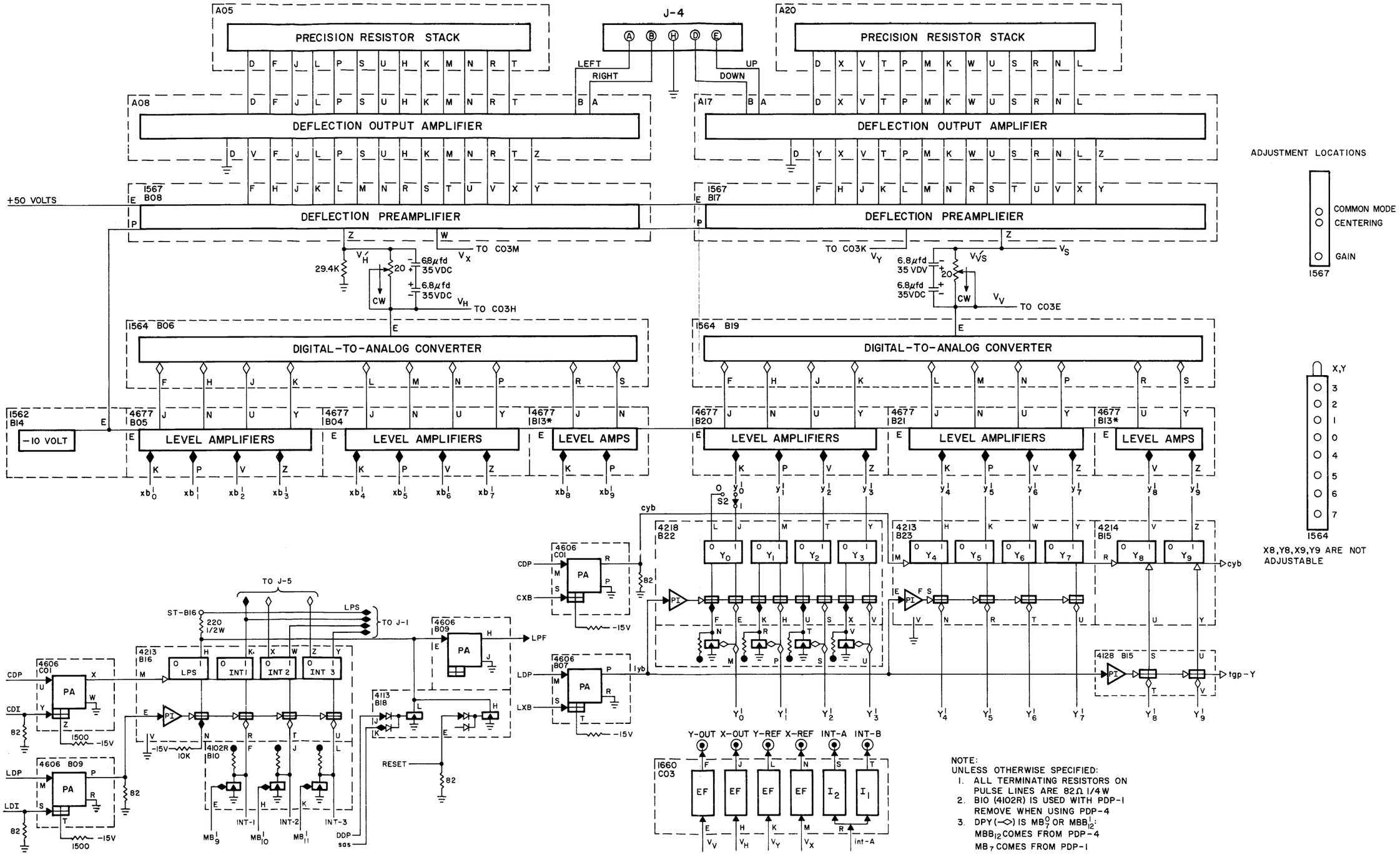


Figure 5-5 Type 30H Display Logic Diagram

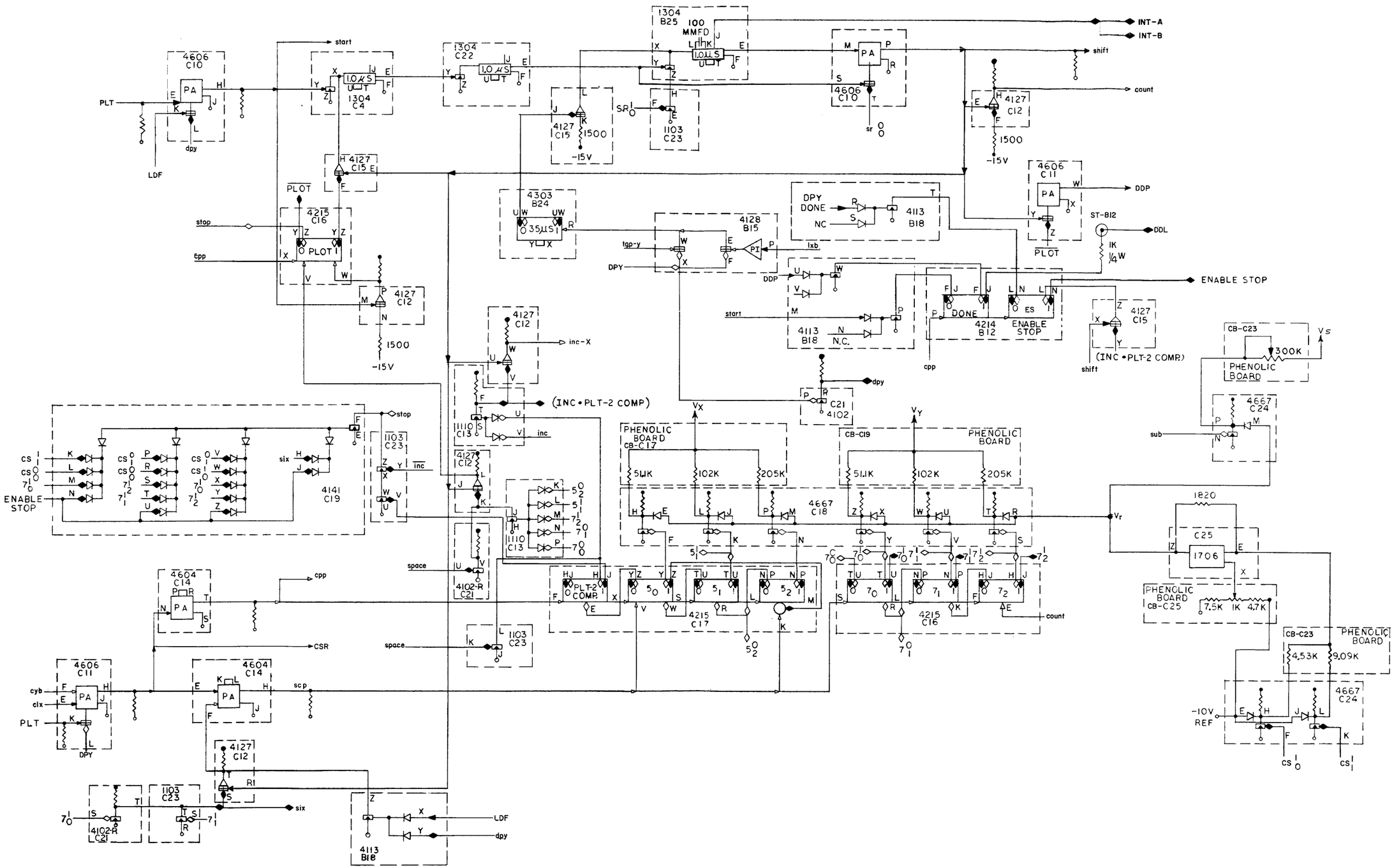


Figure 5-6 Type 30H Symbol Generator Control Logic Diagram

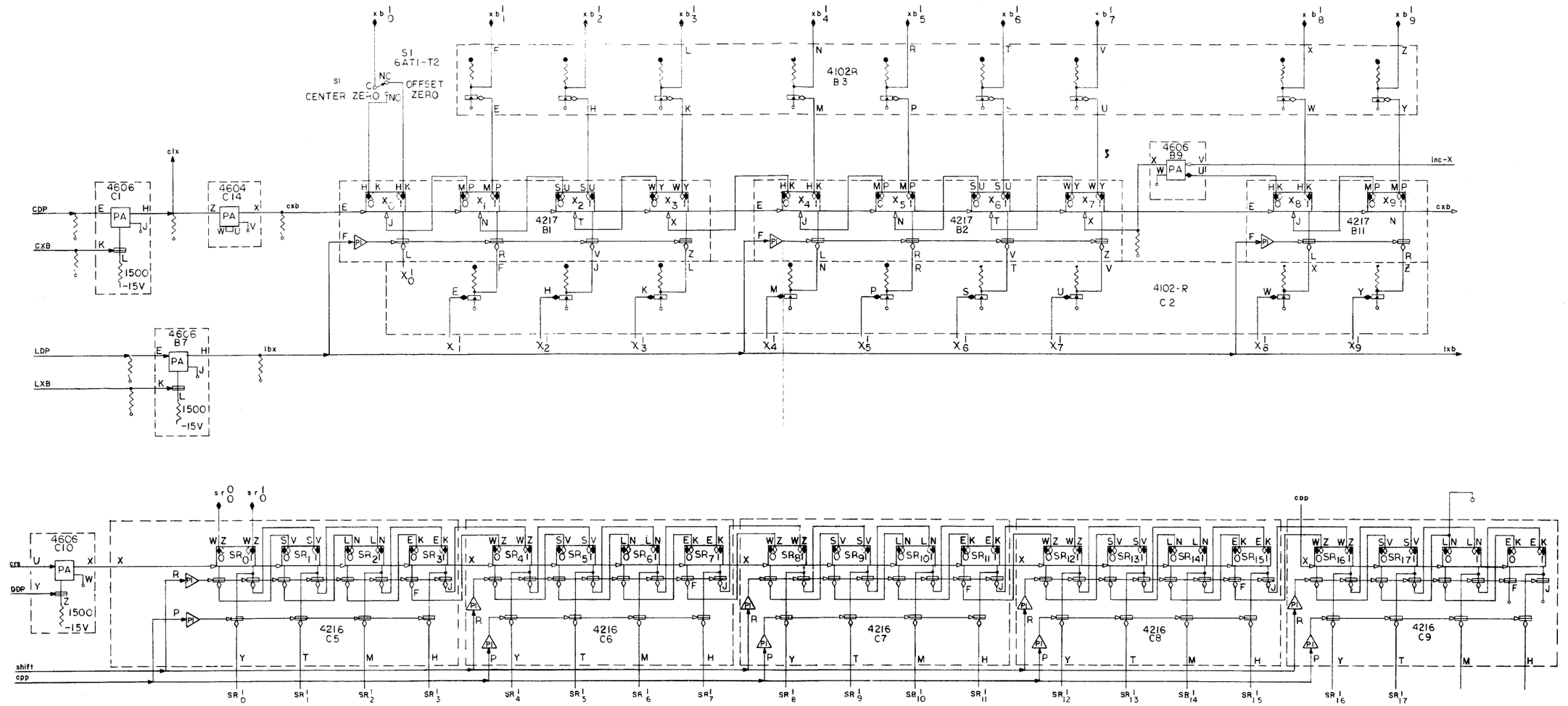
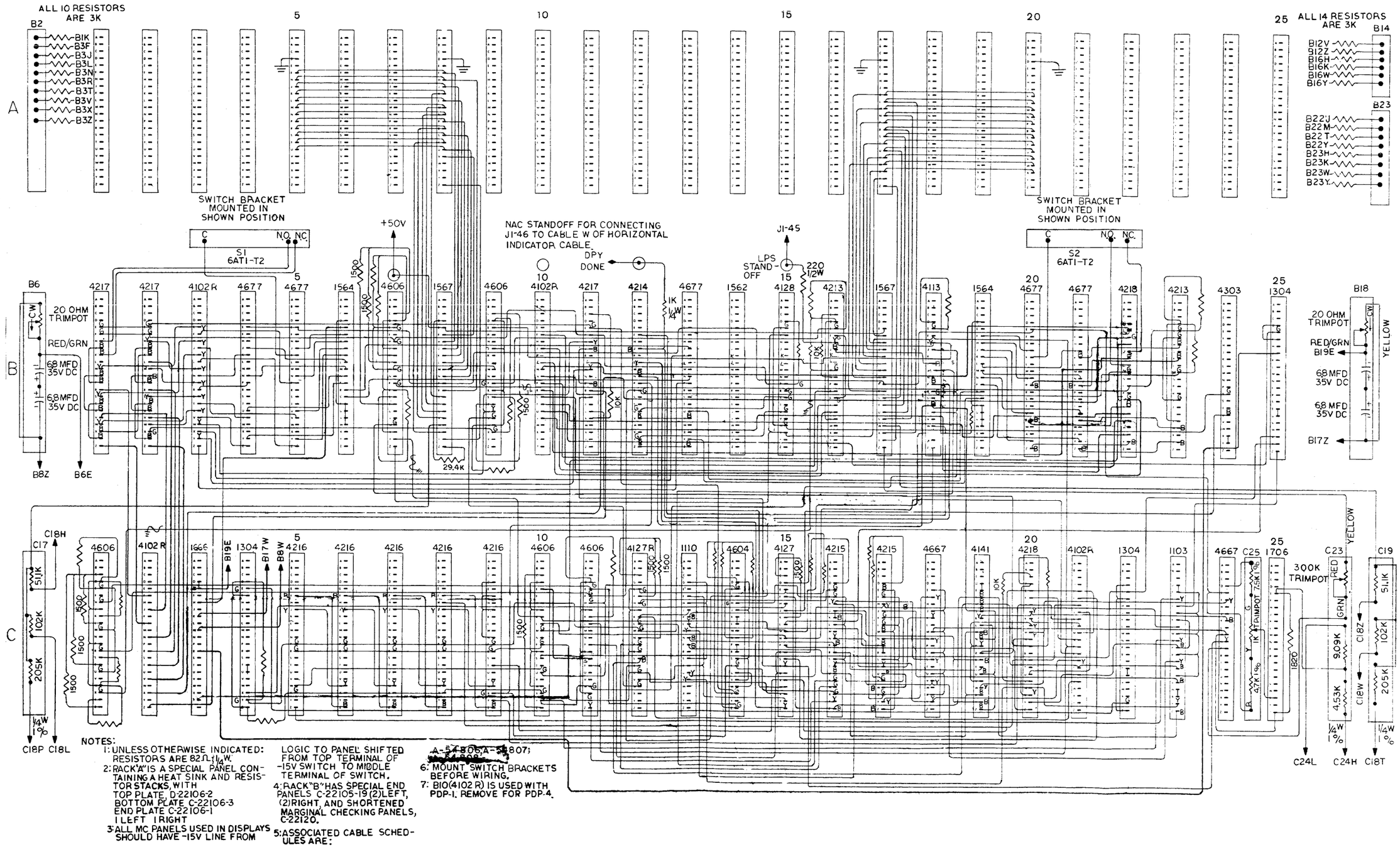


Figure 5-7 Type 30H Symbol Generator Logic Diagram



NOTES:

1: UNLESS OTHERWISE INDICATED: RESISTORS ARE 82Ω 1/4W.

2: RACK "A" IS A SPECIAL PANEL CONTAINING A HEAT SINK AND RESISTOR STACKS, WITH TOP PLATE D-22106-2 BOTTOM PLATE C-22106-3 END PLATE C-22106-1 1 LEFT 1 RIGHT

3: ALL MC PANELS USED IN DISPLAYS SHOULD HAVE -15V LINE FROM LOGIC TO PANEL SHIFTED FROM TOP TERMINAL OF -15V SWITCH TO MIDDLE TERMINAL OF SWITCH.

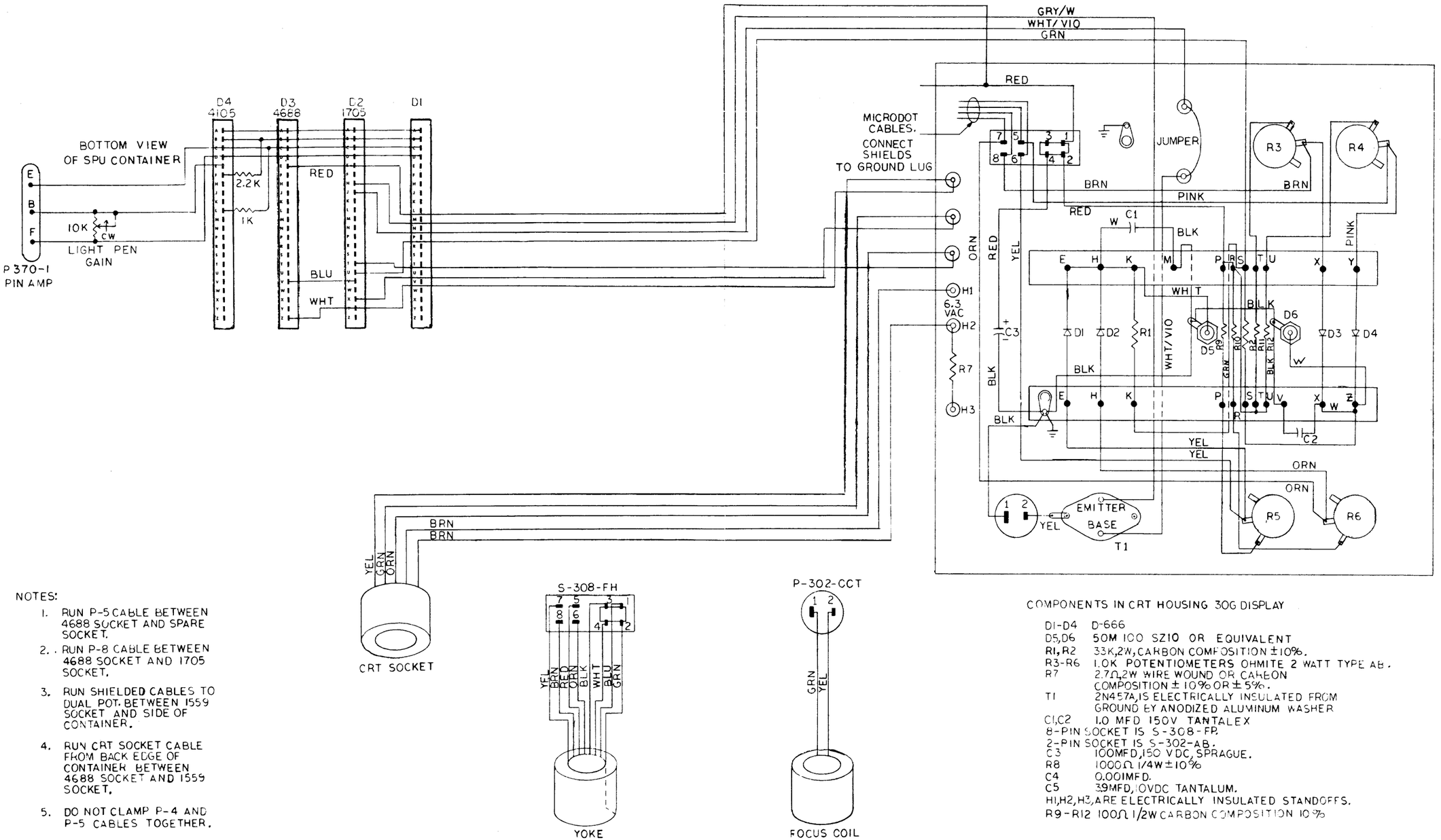
4: RACK "B" HAS SPECIAL END PANELS C-22105-19 (2) LEFT, (2) RIGHT, AND SHORTENED MARGINAL CHECKING PANELS, C-22120.

5: ASSOCIATED CABLE SCHEDULES ARE: A-54805A-54807; 54808

6: MOUNT SWITCH BRACKETS BEFORE WIRING.

7: B10(4102 R) IS USED WITH PDP-1. REMOVE FOR PDP-4.

Figure 5-8 Type 30H Logic Panel Wiring Diagram



NOTES:

1. RUN P-5 CABLE BETWEEN 4688 SOCKET AND SPARE SOCKET.
2. RUN P-8 CABLE BETWEEN 4688 SOCKET AND 1705 SOCKET.
3. RUN SHIELDED CABLES TO DUAL POT. BETWEEN 1559 SOCKET AND SIDE OF CONTAINER.
4. RUN CRT SOCKET CABLE FROM BACK EDGE OF CONTAINER BETWEEN 4688 SOCKET AND 1559 SOCKET.
5. DO NOT CLAMP P-4 AND P-5 CABLES TOGETHER.

CABLE SCHEDULES ARE:

P-4, P-5, P-8 } CS-A-22109 TO 22112

COMPONENTS IN CRT HOUSING 30G DISPLAY

D1-D4	D-666
D5,D6	50M 100 SZ10 OR EQUIVALENT
R1, R2	33K, 2W, CARBON COMPOSITION ±10%.
R3-R6	1.0K POTENTIOMETERS OHMITE 2 WATT TYPE AB.
R7	2.7Ω, 2W WIRE WOUND OR CARBON COMPOSITION ± 10% OR ± 5%.
T1	2N457A, IS ELECTRICALLY INSULATED FROM GROUND BY ANODIZED ALUMINUM WASHER
C1,C2	1.0 MFD 150V TANTALEX
8-PIN SOCKET IS S-308-FP.	
2-PIN SOCKET IS S-302-AB.	
C3	100MFD, 150 VDC, SPRAGUE.
R8	1000Ω 1/4W ± 10%
C4	0.001MFD.
C5	3.9MFD, 10VDC TANTALUM.
H1,H2,H3, ARE ELECTRICALLY INSULATED STANDOFFS.	
R9-R12	100Ω 1/2W CARBON COMPOSITION 10%

Figure 5-9 Type 30 Display Housing Diagram

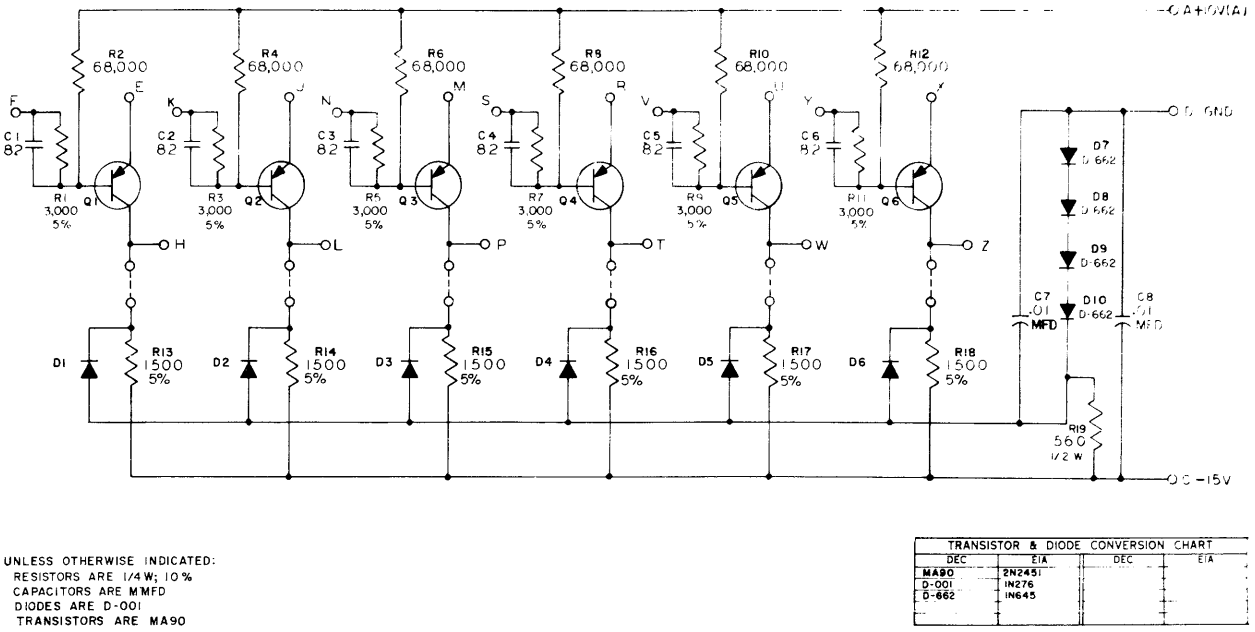


Figure 5-10 Type 1103 Inverter Schematic

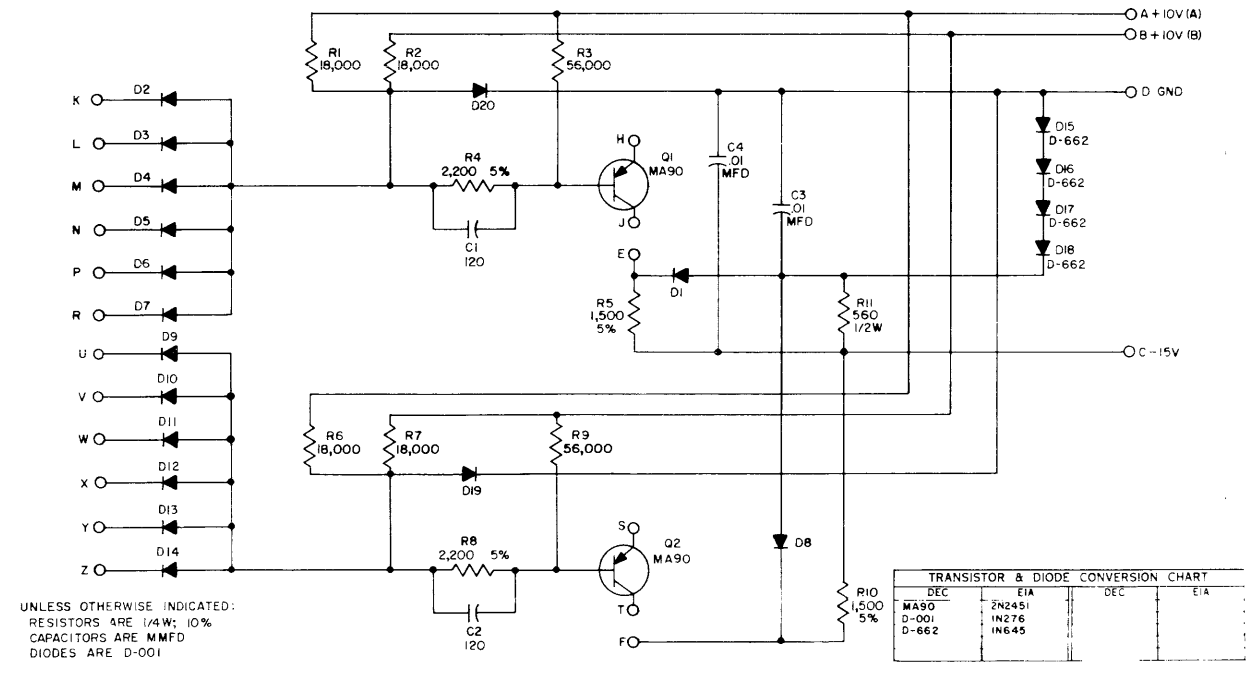


Figure 5-11 Type 1110 Diode Schematic

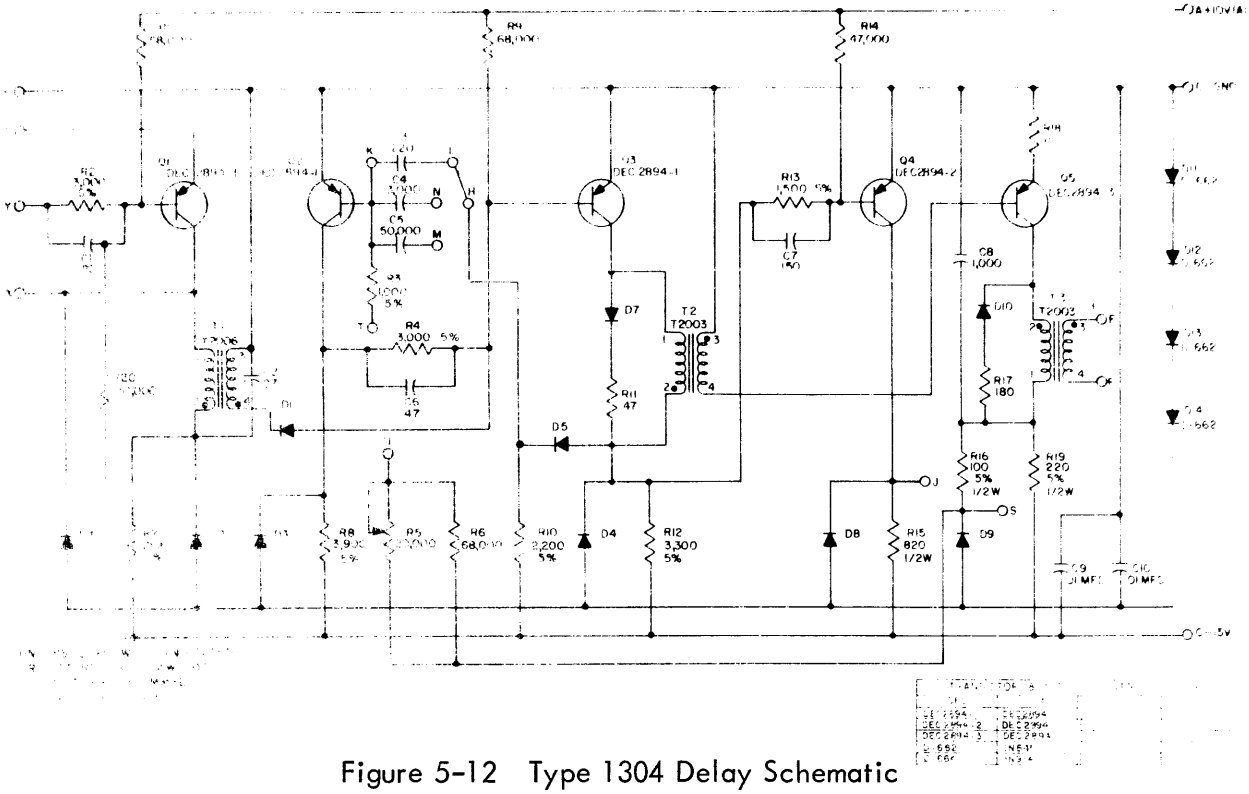


Figure 5-12 Type 1304 Delay Schematic

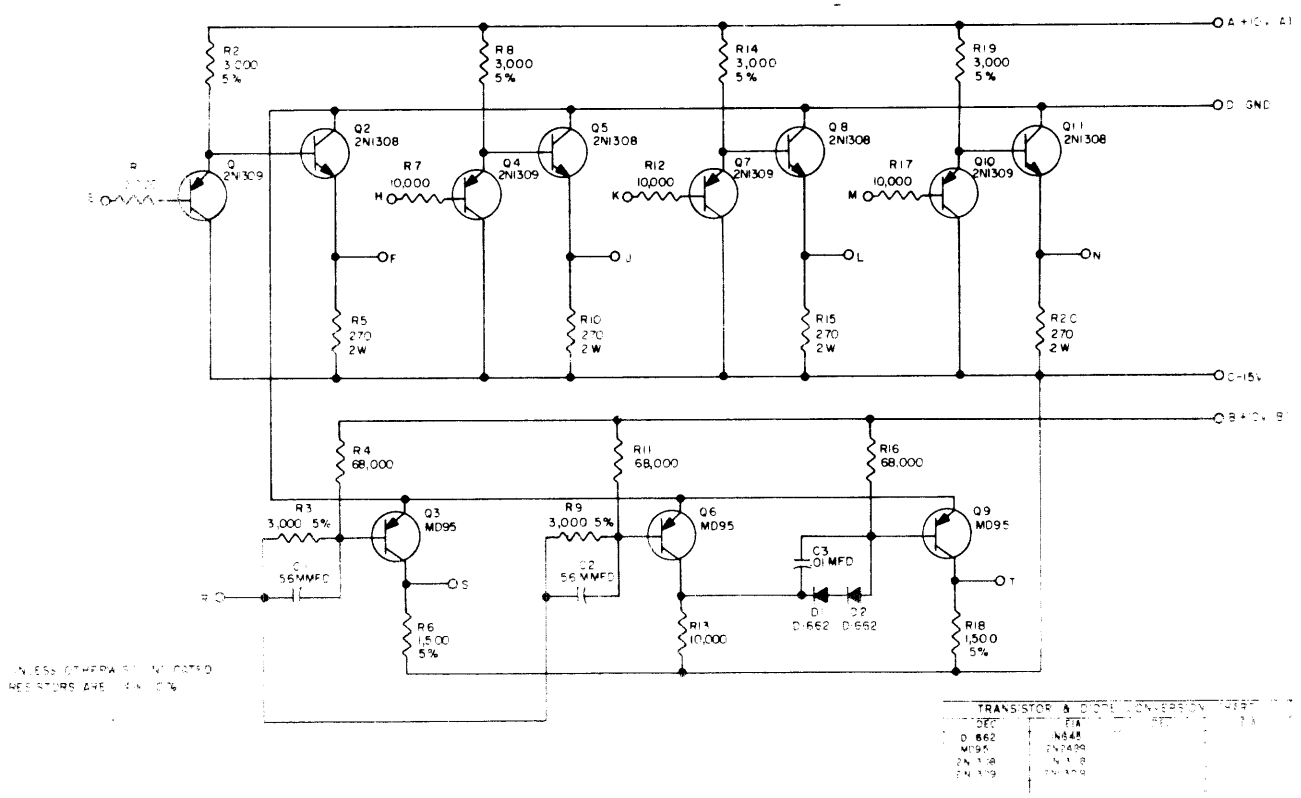


Figure 5-13 Type 1666 Analog Emitter Follower Schematic

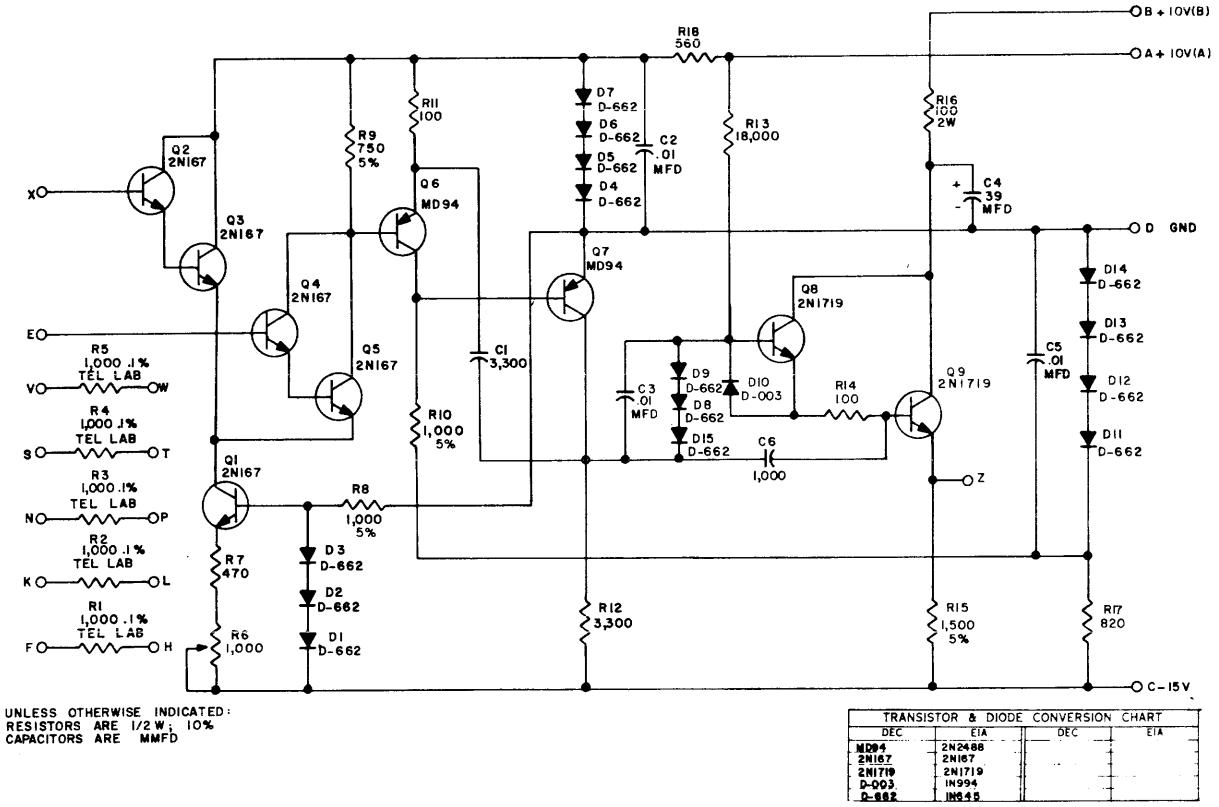


Figure 5-14 Type 1706 Power DC Amplifier Schematic

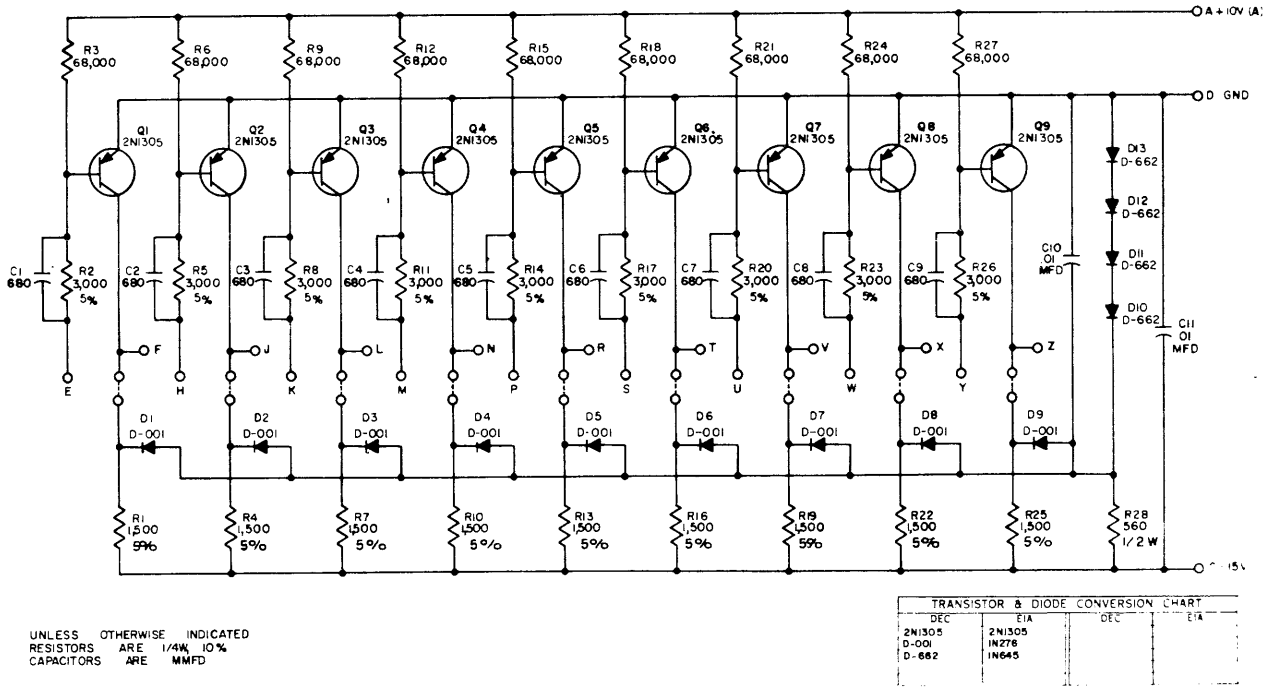


Figure 5-15 Type 4102 Inverter Schematic

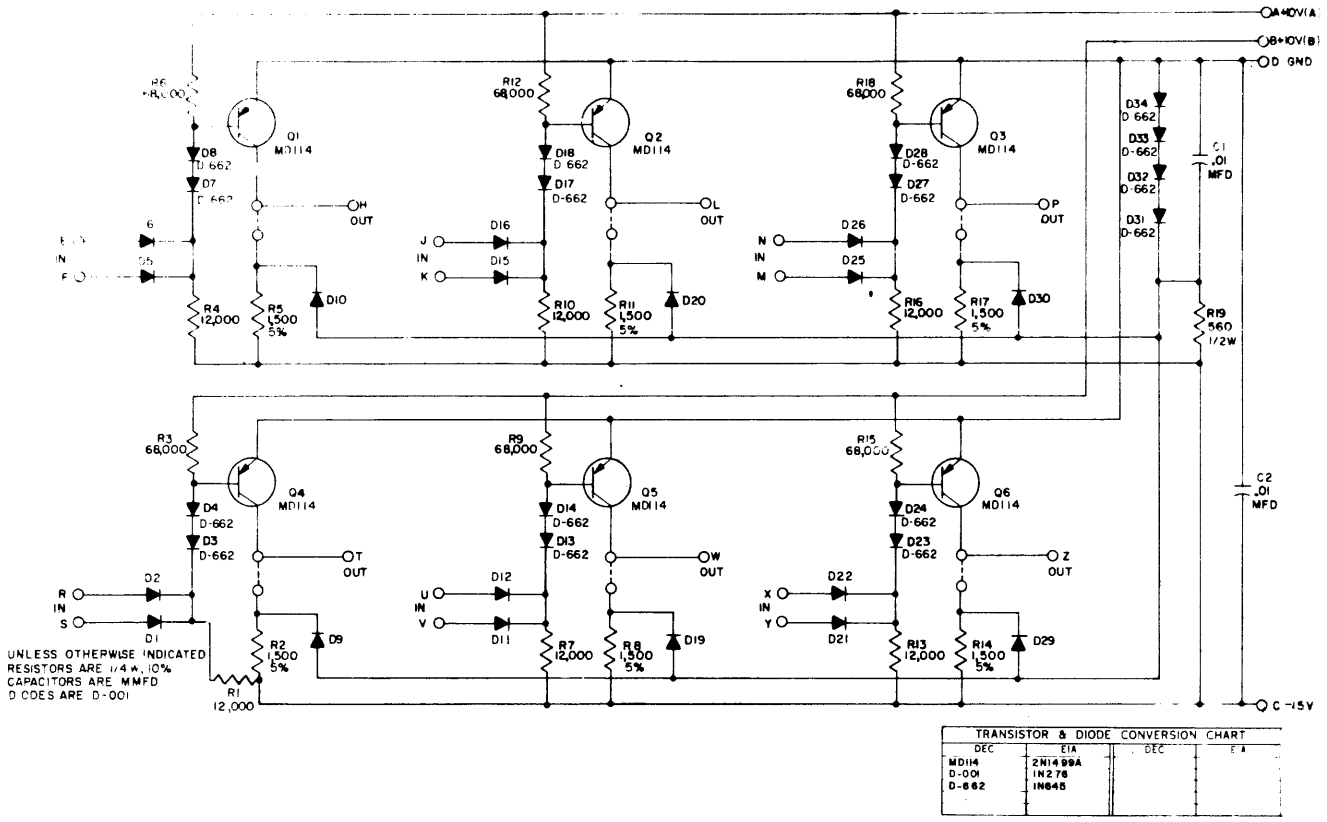


Figure 5-16 Type 4113 Diode Schematic

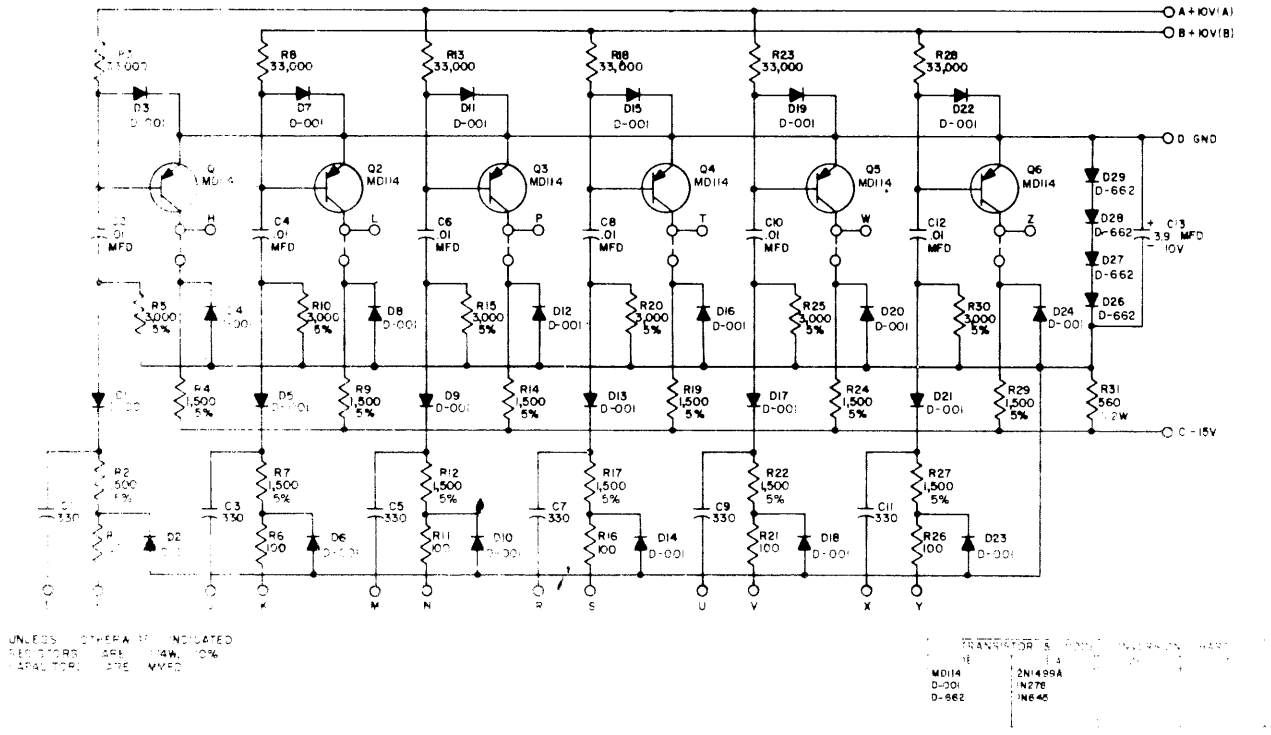


Figure 5-17 Type 4127 Capacitor-Diode-Inverter Schematic

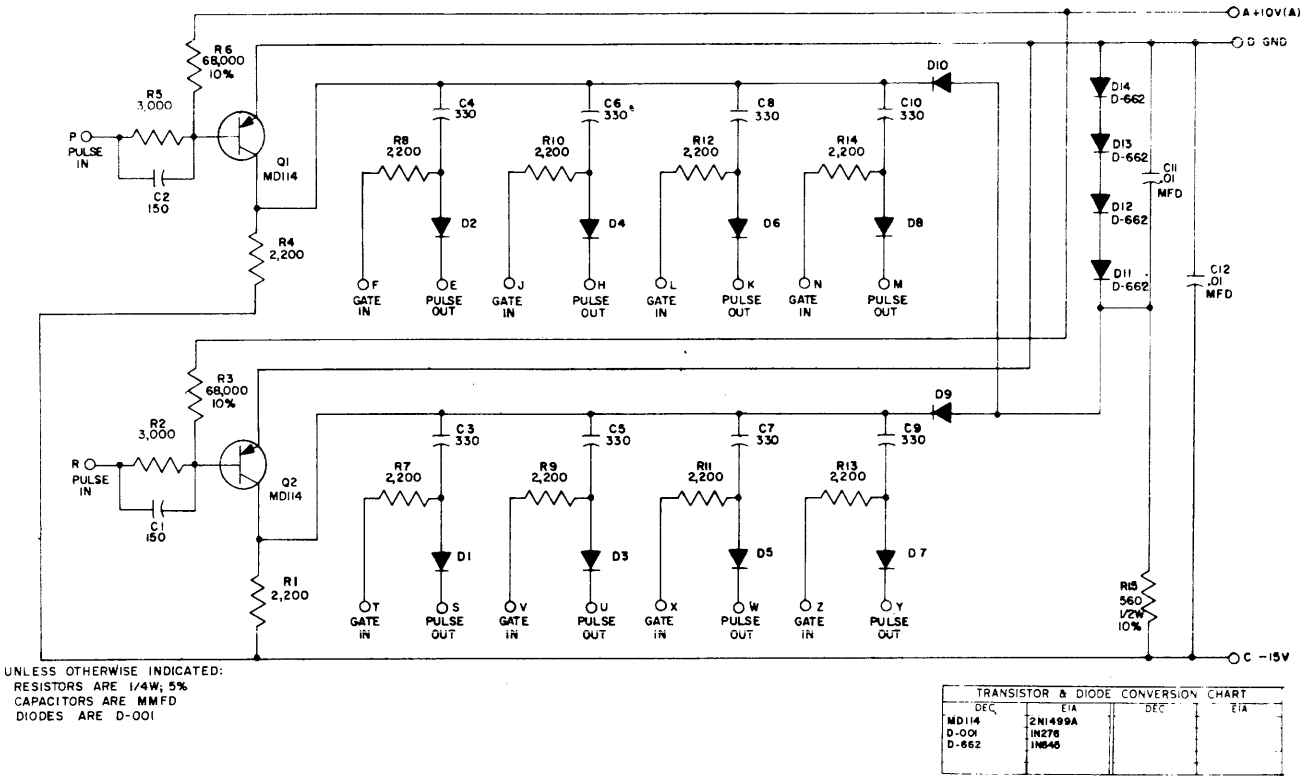


Figure 5-18 Type 4128 Inverter-Capacitor-Diode Schematic

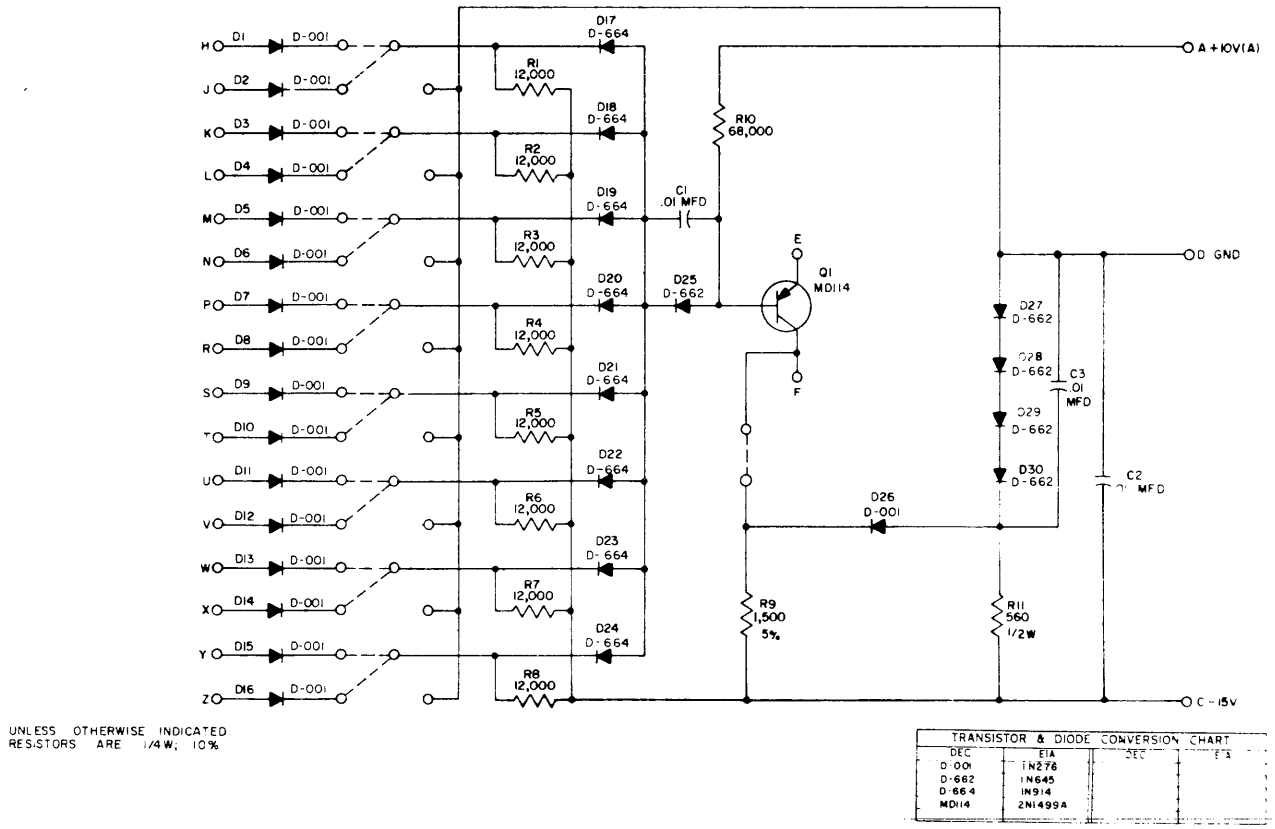
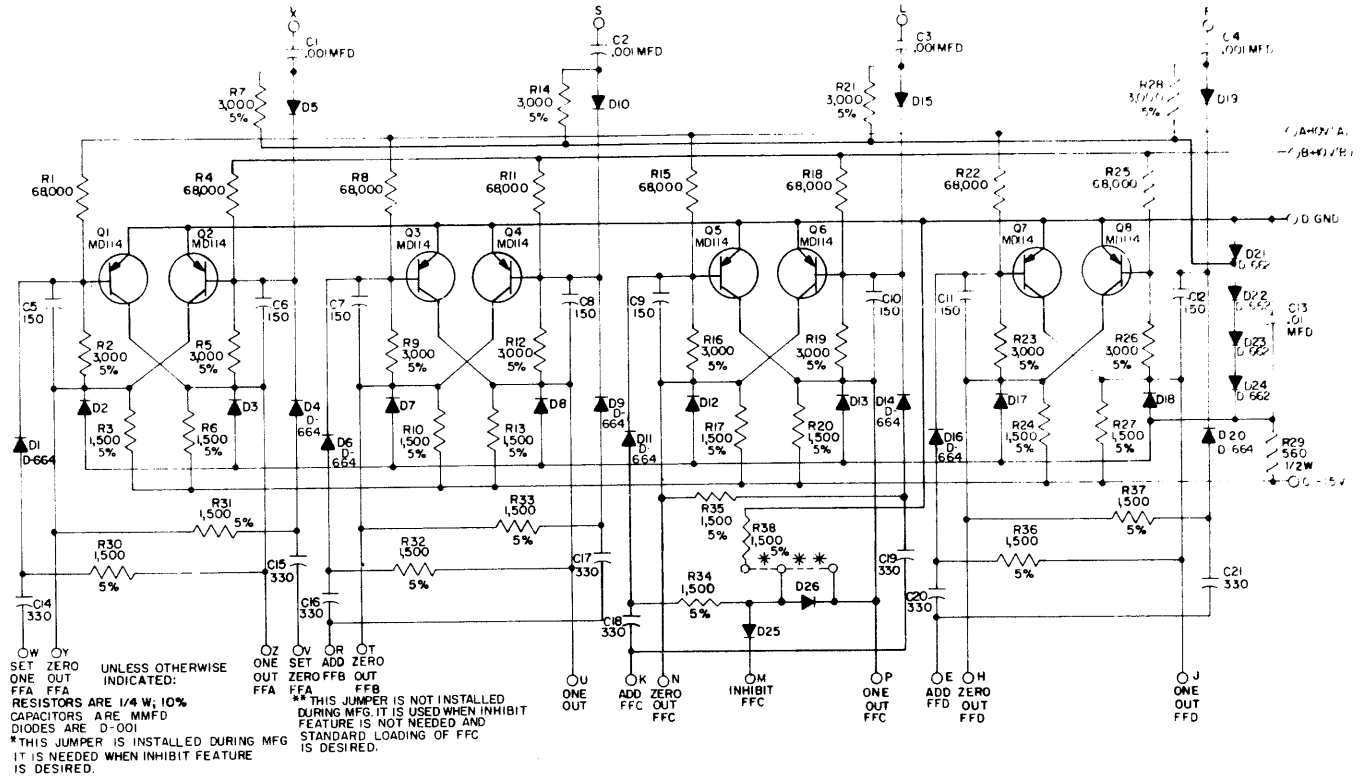
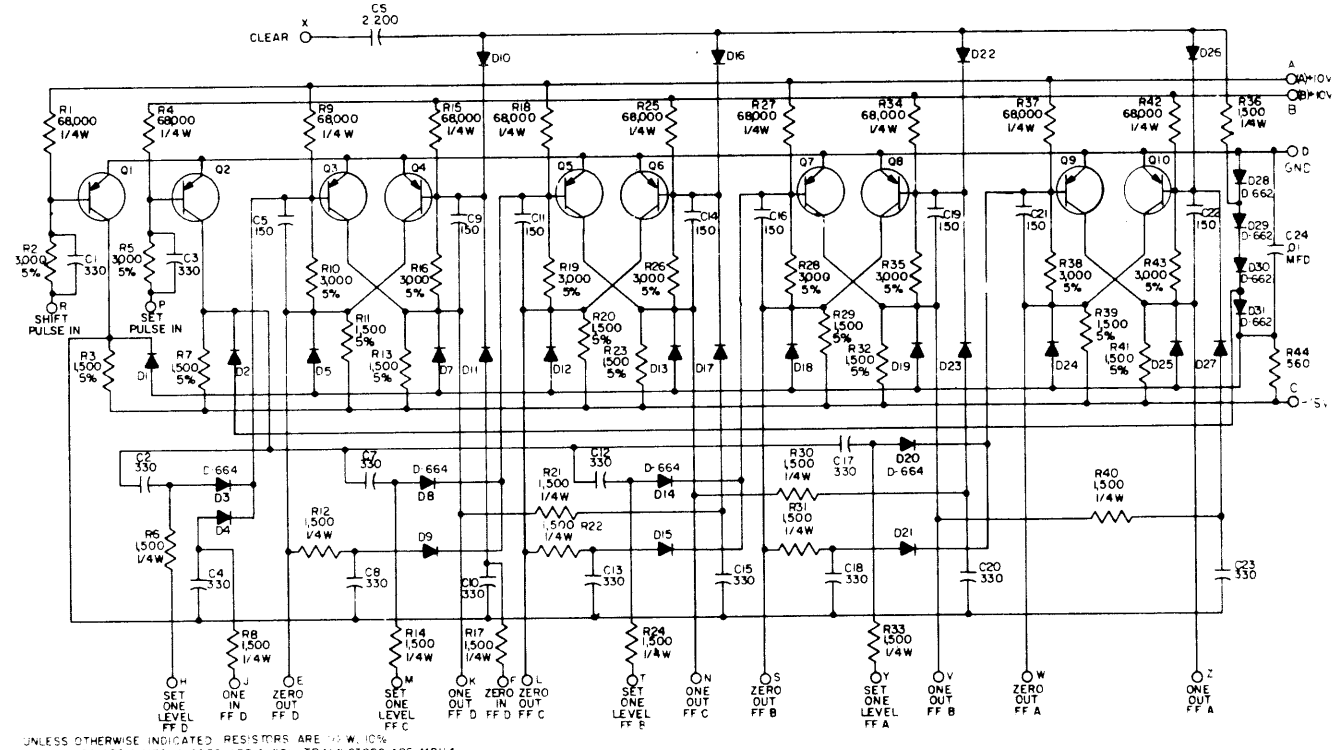


Figure 5-19 Type 4141 Diode Unit Schematic



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MDII4	2N1499A		
D-001	IN276		
D-662	IN645		
D-664	IN914		

Figure 5-20 Type 4215 4-Bit Counter Schematic



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-001	IN276		
D-662	IN645		
D-664	IN914		
MDII4	2N1499A		

Figure 5-21 Type 4216 Quadruple Flip-Flop Schematic

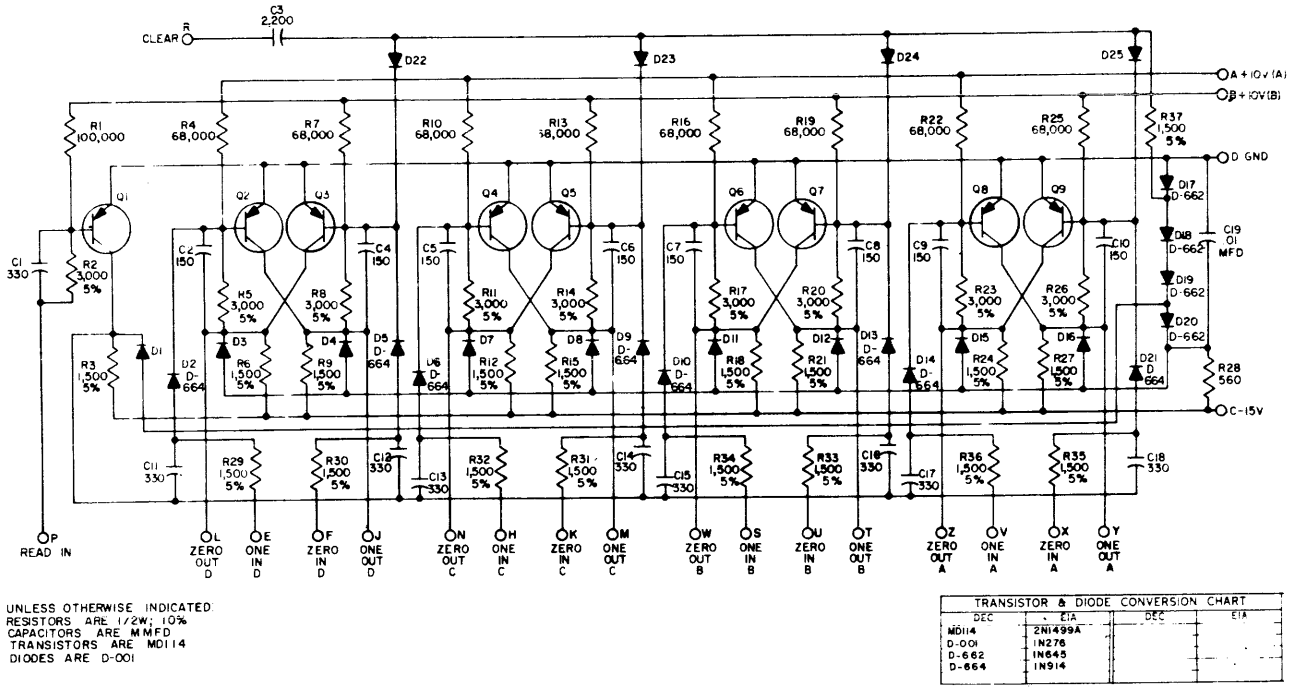


Figure 5-22 Type 4217 4-Bit Counter Schematic

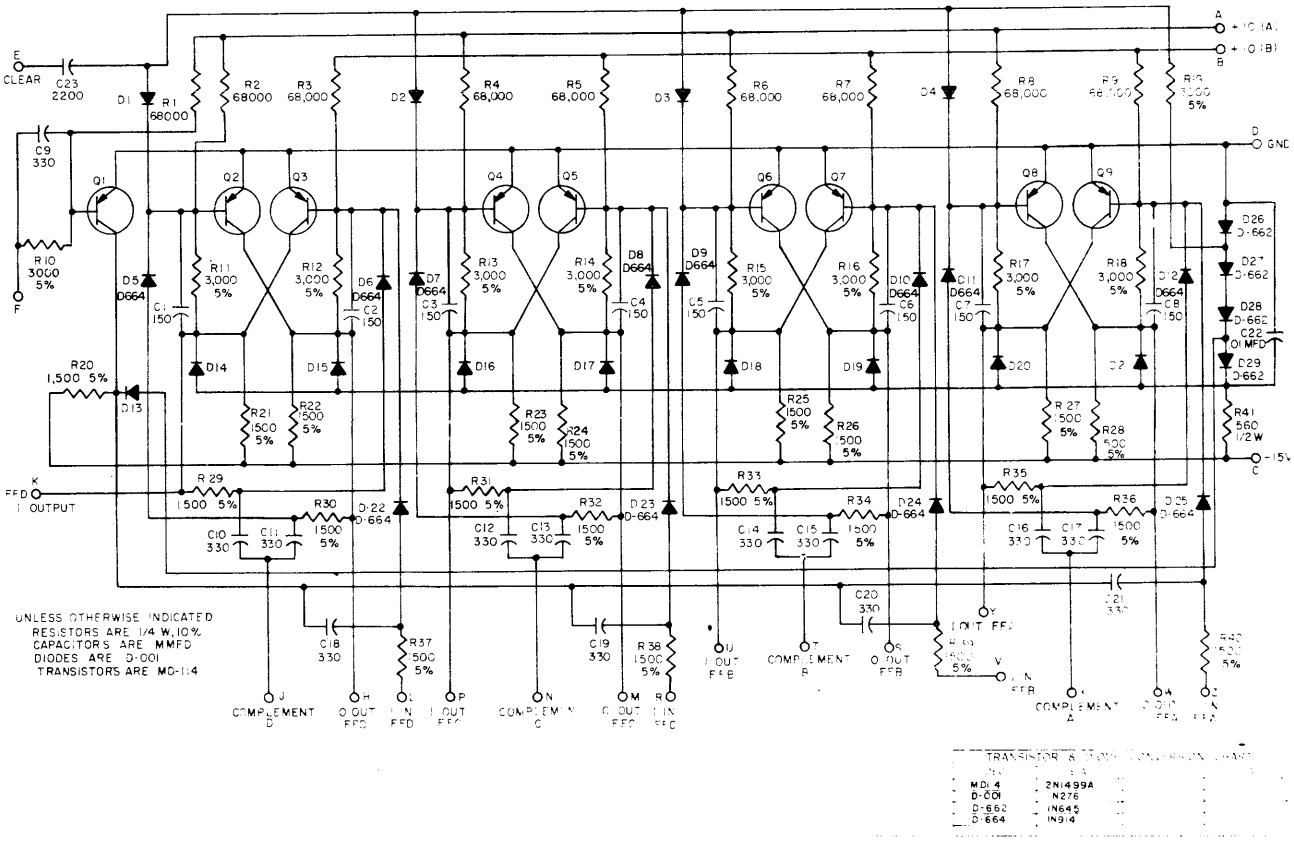
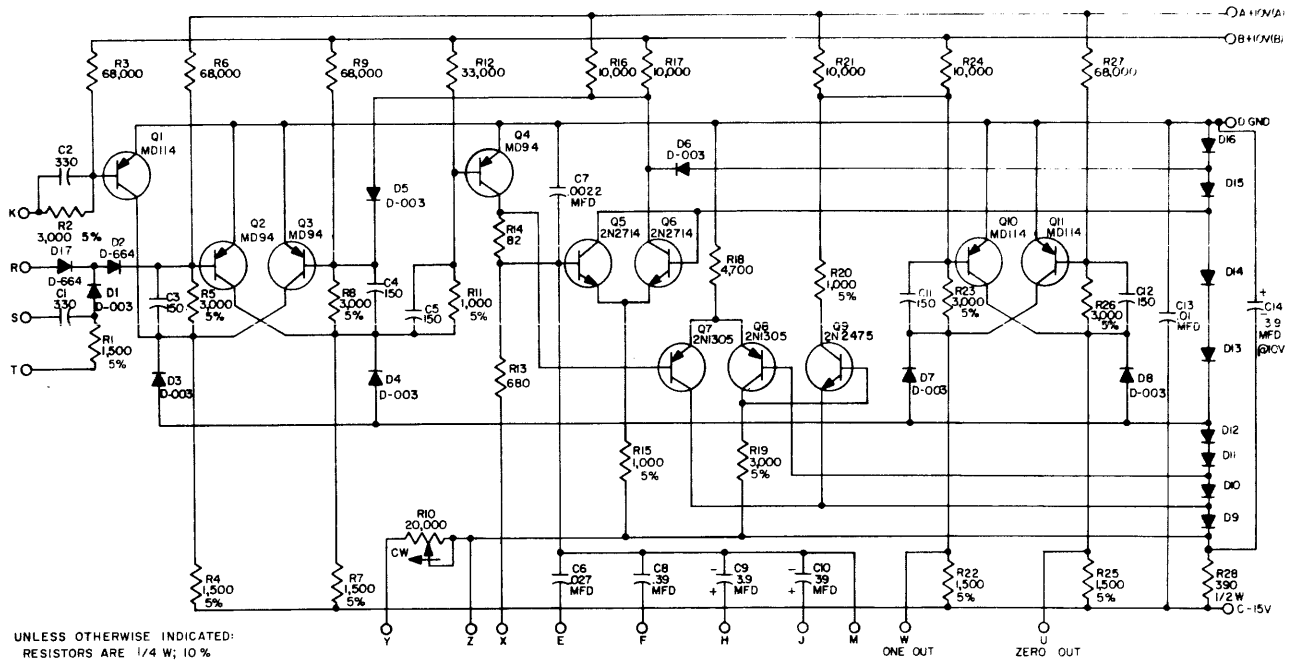
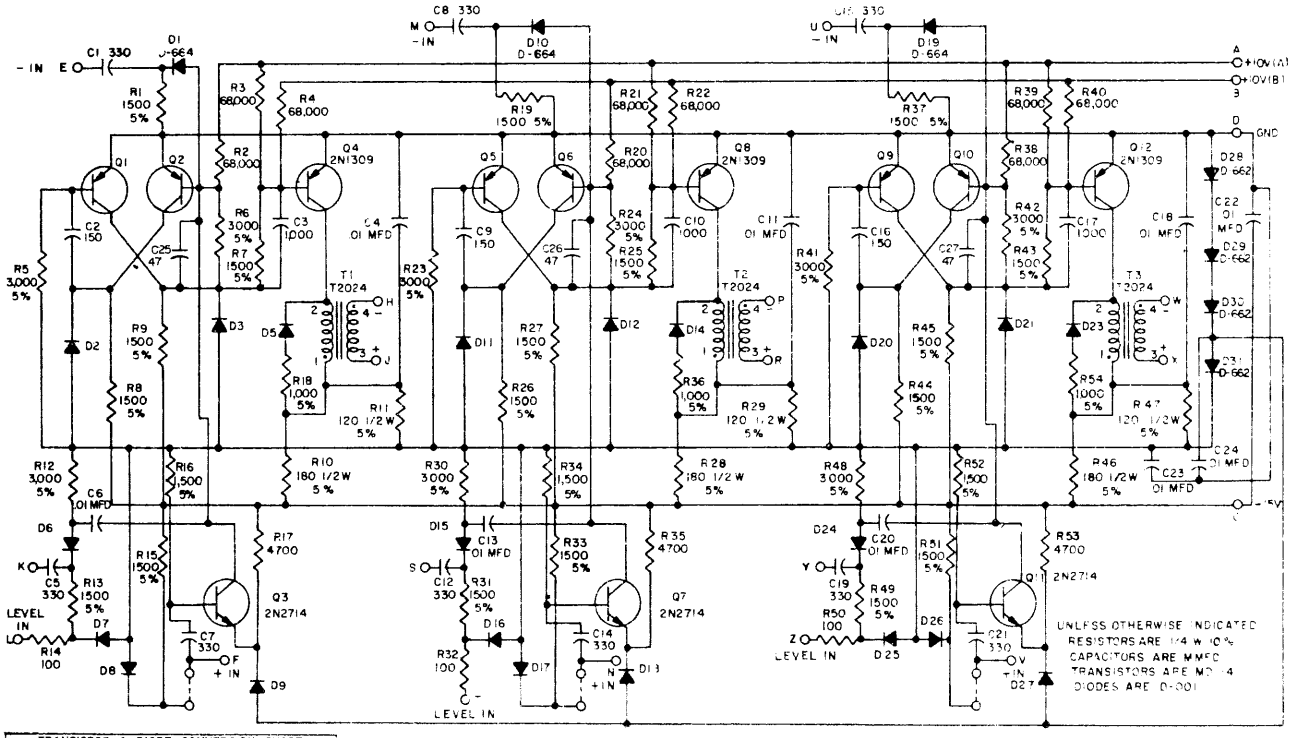


Figure 5-23 Type 4218 Quadruple Flip-Flop Schematic



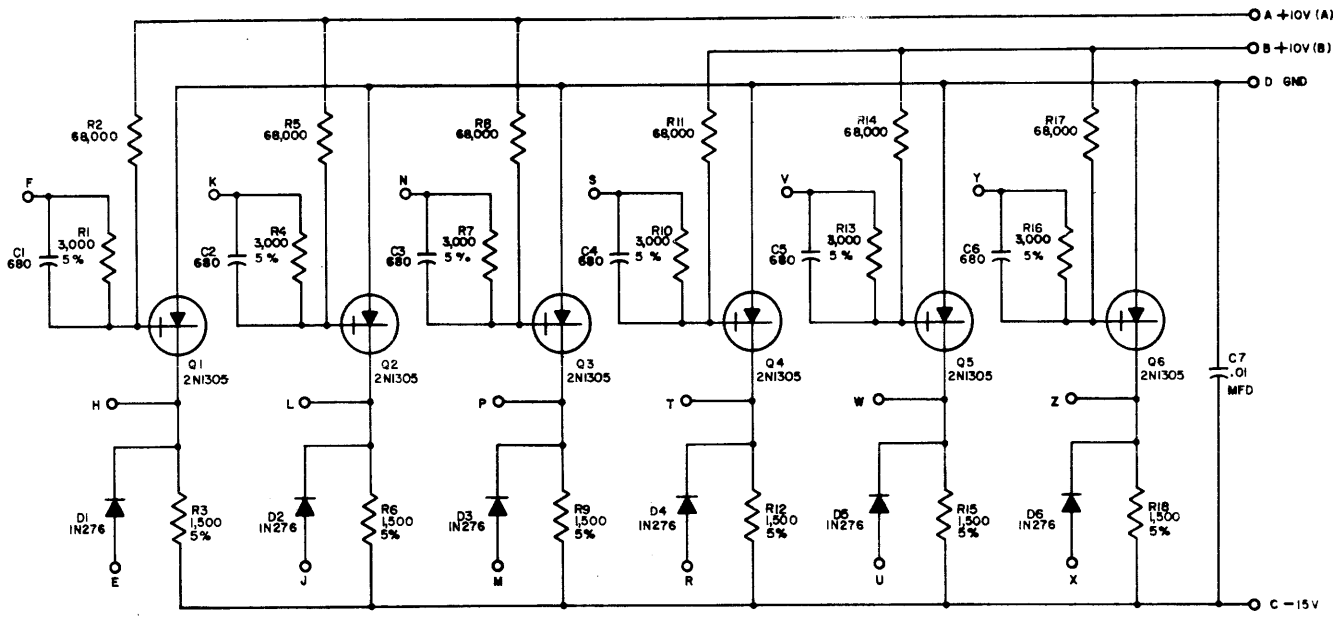
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD94	2N2486	D-662	IN645
MD114	2N1499A	D-664	IN914
2N1305	2N1305	D-003	IN994
2N2475	2N2475		
2N2714	2N2714		

Figure 5-24 Type 4303 Integrating One-Shot Schematic



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A	D-664	IN914
2N2714	2N2714		
2N1309	2N1309		
D-029	IN278		
D-662	IN645		

Figure 5-25 Type 4606 Pulse Amplifier Schematic



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD

Figure 5-26 Type 4667 Level Amplifier Schematic